2015 IEEE North Atlantic Test Workshop

May 11-13, TRADITIONS AT THE GLEN, JOHNSON CITY, NY

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 24th NATW features a general theme of "*Verification and Reliability*."

This year's NATW includes 21 peer reviewed research papers from 6 companies and 9 universities, including 11 student papers which are competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes mini-tutorials on Emulation and Standardization in Test, a Keynote Address on "Warpage as an indicator of reliability" by Prof. Seungbae Park from Binghamton University, an Invited Address on "Outlier treatment of Semiconductor devices – who cares?" by Andy Laidler from ON Semiconductor and a 2nd Keynote Address on "Unique test challenges for compound semiconductor process reliability characterization**"** by Peter Ersland from M/A-COM Technology Solutions. The 2015 workshop is being held at the Traditions at the Glenn Resort and Conference Center, Johnson City, NY and is sponsored by the IEEE Binghamton Section in cooperation with the IEEE Green Mountain Section.

Monday, May 11	
12:00 pm	**Registration**
12:00 - 1:00 pm	**Lunch**
1:00 - 5:00 pm	**Invited Tutorials on Emulation and Standardization in Test** **Tutorial #1:** "Hardware Emulation: The Need for Speed in Test Validation", by Anoop Saha, Mentor Graphics **Abstract:** The rapid growth of hardware emulation has been one of the most disruptive trends of EDA in recent years. This growth is facilitated by the increasingly sophisticated platforms which expand the use cases of emulation much beyond legacy flows. This tutorial will give a brief introduction on emulation and how it enables pre-silicon emulation models to interact and integrate with virtual stimulus. Pre-silicon emulation models are often available many quarters before tapeout and are used in many areas such as OS boot, software driver development, and system stress and performance testing. Increasingly, hardware emulation is used in the development of test contents and to verify the quality of tools and processes used in post-silicon testing. This tutorial will give an overview of how emulators solve the speed challenges in this space keeping intact the full observability, controllability and repeatability. **Tutorial #2:** "IEEE 1687 Basics" by Al Crouch, Asset Intertech **Abstract:** This tutorial is focused on the hardware features and the drivers for 1687 and the resulting tradeoffs. 1687 techniques allow engineering tradeoffs that can result in reduced routing and logic decode; and also allows operational tradeoffs such as concurrent instrument operation and dealing with power domains. The main goal is to enable retargeting, reuse, and instrument portability. **Tutorial #3: "**Overview and Status on P1450.4: Extensions to STIL for Test Flow Specification", Ric Dokken, Roguevation **Abstract:** This tutorial begins by presenting a background of the IEEE 1450 Standard Test Interface Language specification including previous approved extensions to the standard. This background will include examples, identify how commercial tools have adopted the language, and highlight benefits resulting from usage of this language. Focus of the tutorial then moves to the P1450.4 extension, which adds language blocks to define test program flow. New language constructs will be presented in their present pre-ballot state with examples. Explanation of intended applications will include use cases such as online direct consumption by ATE and offline tester retargeting translation tools. The tutorial will conclude with an overview of the challenges faced by the P1450.4 committee, such as how far to go with the extension, and how much impact should be imposed upon previously approved language blocks. It is hoped that this discussion will be interactive and provide feedback that can be shared with the P1450.4 committee.
5:00 - 6:30 pm	**Break**
6:30 - 7:30 pm	**Welcome Reception**
7:30 - 9:00 pm	**Panel Session:** "Verification of Manufacturing Test: (IP Core and SOC)" **Panel Chair/Moderator**: Gene Atwood (IBM) **Panelists**: Alberto Cestero (SRDC), Malinky Ghosh (IBM), Andy Laidler (ON Semiconductor), Ric Dokken (Roguevation), Al Crouch (ASSET InterTech)

Tuesday, May 12

Time	Event
7:00 - 5:00 pm	**Registration**
7:00 - 8:00 am	**Breakfast**
8:00 - 8:10 am	**Opening Remarks:** Paul Reuter, *General Chair*
8:10 - 8:55 am *Introduction by Krishna Chakravadhanula, Program Chair*	**Keynote Address:** “Warpage as an indicator of reliability” by Prof. Seungbae Park, Opto-Mechanics and Physical Reliability Laboratory, Binghamton University **Abstract:** Electronics components and their assembly reliability is assessed in various stages with numerous methods. Among them, warpage is a primary indicator of addressing reliability of the life time as well as discovering potential problems during assembly processes. Primary cause of the warpage, methods of testing, and solutions are discussed.
8:55 - 9:40 am *Introduction by Nicola Nicolici, Program Vice-Chair*	**Invited Address:** “Outlier Treatment of Semiconductor Devices – Who Cares?” by Andy Laidler, ON Semiconductor **Abstract:** Semiconductor device populations for Cpk reports which include “outlier” devices present the problem of disposition and this treatment of various outliers often leads to the question “Was the outlier predicted by simulation?” Methods and approaches to identify different types of outliers beyond guard-banded test limits include graphical analysis and interpretation of digital test distributions, multi-variable test correlations, Iddq and Voltage Screen failure modes and stresses the manner in which devices behave to help establish methods for disposition. A qualitative assessment and findings of outlier behavior is presented by example and it is suggested to occur prior to the testing of qualification material to help reduce the opportunity for failures to occur during the Qualification Phase requiring formal disposition.
9:40 - 9:50 am	**Coffee Break / Reception**
9:50 - 10:50 am	**Student Session 1: Reconfigurable Logic for Test, Validation and Fault Tolerance** **Session Chair:** Prathima Agrawal, Auburn University
9:50 - 10:10am	*Yi Sun (SMU, US)*: Using an FPGA in a 3D Stacked IC to Prevent LSIB Bitstream Snooping
10:10 - 10:30am	*Pouya Taatizadeh (McMaster Univ., Canada)*: An Emulation Infrastructure for Improving the Accuracy of Assertion-Based Bit-Flip Detection in Post-Silicon Validation
10:30 - 10:50am	*Ramtin Zand (Univ. of Central Florida, US)*: Adaptive Mitigation of Radiation-Induced Errors and TDDB in Reconfigurable Logic Fabrics
10:50 - 11:00 am	**Break**
11:00 - 12:00 pm	**Student Session 2: Concurrent Test** **Session Chair:** Jennifer Dworak, Southern Methodist University
11:00 - 11:20am	*Baohu Li (AuburnU, US)*: Multivalued Logic for Reduced Pin Count and Multi-site SoC Testing
11:20 - 11:40am	*Qutaiba Khasawneh (SMU/Oncor, US)*: An Industrial Case Study: PaRent (Parallel & Concurrent) Testing for Complex Mixed-Signal Devices
11:40 - 12:00pm	*Huiting Zhang (AuburnU, US)*: SoC TAM Design to Minimize Test Application Time
12:00 - 1:15 pm	**Lunch**
1:15 - 2:15 pm	**Student Session 3: Debugging and ATPG** **Session Chair:** Alberto Cestero, IBM
1:15 - 1:35pm	*Amin Vali (McMaster Univ., Canada)*: Satisfiability-Based Analysis of Failing Traces During Post-Silicon Debug
1:35 - 1:55pm	*Swati Chakraborty (Texas A&M, US)*: At-Speed Path Delay Test
1:55 - 2:15pm	*Micah Thornton (SMU, US)*: Intelligent Targeting of Cell-Aware Type Faults using Mandatory Conditions for Detection
2:15 - 2:30 pm	**Break**
2:30 - 3:30 pm	**Student Session 4: Beyond the Digital Test Frontier** **Session Chair:** Ted Cooley, Cooley & Company
2:30 - 2:50pm	*Nicholai L’Esperance (UVermont, US)*: OFDM Multi-tone Signal Generation Technique for Analog Circuitry Test Characterization
2:50 - 3:10pm	*Aydin Dirican (UMass Lowell, US)*: A CMOS built-in RMS detector for power supply ripple testing
3:10 - 3:30pm	*Muhammad Abbas Choudhary (NAMAL College/Univ. of Engineering & Technology, Pakistan)*: Identification and Management of Risk in Software Engineering Projects

Time	Event
3:30 - 3:45 pm	**Break**
3:45 - 4:45 pm	**Paper Session 1: Test and Validation Advances** **Session Chair:** Vivek Chickermane, Cadence
3:45 - 4:10pm	*Ramesh Tekumalla (Avago, US)*: Clock Domain Imbalances and their Impact on Test Architecture
4:10 - 4:35pm	*Carl Wisnesky (Cadence, US)*: 2-Pin Test with Overlapped Scan Using Manchester Encoding
4:35 - 5:00pm	*Mohamed Hanafy (Mentor Graphics/Ain Shams Univ., Egypt)*: Complete Properties Extraction from Simulation Traces for Assertions Auto-Generation
5:00 - 6:30 pm	**Break**
6:30 - 9:30 pm	**Social Event: Banquet and Best Student Paper Award and Murder Mystery Show** (Location: Traditions at the Glen, Johnson City, NY)
	Wednesday, May 13
7:30 - 12:00 pm	**Registration**
7:30 - 8:30 am	**Breakfast**
8:30 - 9:15 am *Introduction by Vishwani Agrawal, Auburn Univ.*	**Wednesday Keynote Address: "**Unique test challenges for compound semiconductor process reliability characterization**"** by Peter Ersland, Sr. Principal Engineer, M/A-COM Technology Solutions **Abstract:** This presentation will describe the tools and techniques implemented to address unique device characterization challenges, focusing on compound semiconductor technologies used for high speed, high power RF and microwave frequency applications.
9:15 - 10:30 am	**Paper Session 2: Hierarchical Test** **Session Chair:** Ramesh Tekumalla, Avago Technologies
9:15 - 9:40am	*Kelly Ockunzzi, Brion Keller (IBM/Cadence, US)*: Divide and Conquer: Testing Chips Hierarchically
9:40 - 10:05am	*Yu Huang (Mentor Graphics, US)*: Hybrid Hierarchical and Modular Tests for SoC Designs
10:05 - 10:30am	*Christos Papameletis (Cadence/IMEC, US)*: At-Speed Testing of Inter-Die Interconnects in 2.5D- and 3D-SICs
10:30 - 10:40 am	**Break**
10:40 - 11:55 am	**Paper Session 3: Failure Diagnosis and Power-Aware Test** **Session Chair:** Mike Vachon, Cadence
10:40 - 11:05am	*Yu Huang (Mentor Graphics, US)*: Case Studies of Silicon Debug by Scan-Based Diagnosis
11:05 - 11:30am	*Joe Swenton (Cadence, US)*: A Novel Failure Diagnosis approach for Low Pin Count and Low Power Compression Architectures
11:30 - 11:55am	*Ramesh Tekumalla (Avago, US)*: Scan Power Reduction Using Clock Domain Suppression
11:55 - 12:00 pm	**Closing Remarks**, Paul Reuter
12:00 - 1:00 pm	**Lunch and Program Committee Meeting (Valley View Tent)**

** denotes presenter*