2010 IEEE NORTH ATLANTIC TEST WORKSHOP

MAY 12-14, LE CHAMBORD, HOPEWELL JUNCTION, NY 12533

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient testing methodologies and designs. With the increasing complexity in both design and test of integrated circuits and systems, the **19th NATW** features the theme: *"Economics: The Dirtiest Word in Test"* and a **Panel** dedicated to Intellectual Property. This year, NATW includes 21 papers from 5 different companies and 8 different universities, including 10 student papers competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes a **Keynote Address** on Complexity in High-end Processor Design, a 1st Invited Address on Soft Errors, and a 2nd Invited Address on A Design Automation Tool Flow for DFT. The 2010 workshop is held at Le Chambord in Hopewell Junction, NY and is sponsored, in part, by the Green Mountain Section of IEEE. NATW corporate / academic supporters for 2010 include Mentor Graphics, SynTest Technologies, Auburn University Wireless Engineering Research & Education Center, and the Vermont chapter of IEEE Solid State Circuits Society.

Wednesday, May 12	
6:30 - 7:30pm	**Welcome Reception and Registration**
7:30 - 9:00pm	**Panel Session:** "Intellectual Property: .edu, .com and .gov". Panel Chair: Gene Atwood (IBM) **Panelists**: George Kachen (Univ. of Massachusetts), C.J. Clark (Intellitech), Jim Brown (IBM), George Doerre (IBM), Dean Adams (Aardvark Intellex), Sonny Maynard (The Pentagon)
Thursday, May 13	
7:30 - 8:00am	**Breakfast**
8:00 - 8:15am	**Opening Remarks:** Linda Milor, *General Chair*
8:15 - 9:00am *Introduction by Vikram Iyengar, Program Co-Chair*	**Keynote Address:** "Growing System Complexity in High-end Processor and System Design" by Leon Stok (IBM) **Abstract:** At IBM, we have dramatically shortened the time-to-market for our High-end Processor and System designs. By looking at the entire design process from concept design to final test and validation, many of the steps have been improved and the complete development schedule shortened by 35%. In this presentation, we will look at the lessons learned and techniques applied to accomplish this.
9:00 - 9:45am *Introduction by Jennifer Dworak, Program Co-Chair*	**First Invited Address:** "Soft Errors Make Hard Problems for Chip Designers" by John Hayes (Univ. Michigan) **Abstract:** The steady shrinking of the transistors used in IC chip manufacture makes them increasingly vulnerable to soft errors caused by external radiation or by internal process variations. This talk will briefly review the major sources and impact of soft errors. It will describe some recent methods to model them and to analyze their effects on digital circuit behavior and reliability.
9:45 - 10:00am	**Coffee Break / Reception**
10:00 - 11:15am	**Student Session 1: Design-For-Test,** Session Chair: TBD
	1.1 A New Algorithm for Post-Silicon Clock Measurement and Tuning. Z. Lak* and N. Nicolici (McMaster Univ.) 1.2 A "Recycling"-Based DFT Methodology Approach: A Case of Power Management ICs. Kemal Kulovic* and Martin Margala (U. Mass. - Lowell) 1.3 Design and Analysis of an Adaptive X-Tolerant XOR Compactor with Controllable Fan-out. Samah Mohamed Saeed* and Ozgur Sinanoglu (Kuwait University)
11:15 - 11:30pm	**Networking Break**
11:30 - 12:30pm	**Lunch**
12:30 - 1:45pm	**Student Session 2: Diagnosis And Test Pattern Generation,** Session Chair: TBD
	2.1 Max-Fill: A Method to Generate High Quality Partially-functional Broadside Delay Tests. Xiaoxin Fan*, Sudhakar M. Reddy (Univ of Iowa) and Irith Pomeranz (Purdue) 2.2 A Diagnostic Test Generation System. Yu Zhang* and Vishwani D. Agrawal (Auburn Univ.) 2.3 Dynamic Test Set Selection using Implication-Based On-Chip Diagnosis. Nicholas Imbriglia*, Nuno Alves and Jennifer Dworak (Brown Univ.)
1:45 - 3:00pm	**Student Session 3: Analog Test And Defect Modeling,** Session Chair: TBD
	3.1 Ring-Oscillator Based Time Amplifier for Improved Testability of High Speed Signals. Kemal Kulovic* and Martin Margala (U. Mass – Lowell) 3.2 Detecting Shorts And Open Faults In A Mask Using Lithography Simulation. Lokesh Subramany*, Rance Rodrigues and Sandip Kundu (U. Mass – Amherst) 3.3 Low Overhead Soft Error Detection And Correction Scheme For High Performance Pipelined Data Paths. Sohan Purohit*, Sai Rahul Chalamalasetti and Martin Margala (U. Mass – Lowell)
3:00 - 3:15pm	**Coffee Break**

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3:15 - 4:30pm	**Session 4: Diagnosis,** Session Chair: TBD
	4.1 Using Scan Patterns Alone for Chain Diagnosis. Yu Huang* (Mentor Graphics) 4.2 A Complete Test and Diagnostic System for Caches for Fault Tolerant Systems. Fahad Ahmed and Linda Milor* (Georgia Institute of Tech.) 4.3 Diagnosis of Multiple Defects on Scan Enable and Clock Trees. Yu Huang*, Liyang Lai, Ruifeng Guo and Wu-Tung Cheng (Mentor Graphics)
6:00 pm	**Social Program (Banquet at Le Chambord) and Best Student Paper Award**
Friday, May 14	
7:30 - 8:00am	**Breakfast**
8:00 - 8:45am *Introduction by Martin Margala, General Vice-Chair*	**Second Invited Address:** "Front-to-Back Design Automation Tool Flow" by Dave Lackey (IBM) Abstract: At the 32 nm technology node, IBM has made major changes in its Design for Testability architecture and tool flow, including converting from LSSD to Mux-scan, and supporting a fully hierarchical DFT synthesis flow. In incorporating this set of changes, IBM has worked within its own internal EDA organization, as well as with its 3rd-party EDA partners, to provide a new design flow that achieves fully automated and high quality DFT insertion, at-speed test, Array BIST and repair, and testing of embedded high-speed and mixed signal IP.
8:45 - 10:00am	**Session 5: Invited Special Session on Solid State Circuits & Systems Test,** Session Chair: Pascal Nsame (IBM)
	5.1 Statistical Approach for Yield Optimization for Minimum Energy Operation. Khan Nomani* (Univ. of South Carolina, Columbia) 5.2 Memory Redundancy Analysis using Critical Area Analysis. Simon Favre* (Mentor Graphics) 5.3 Design-for-Reliability of 45 nm SOI Semiconductor SoCs with Integrated eDRAM. Pascal Nsame* (IBM)
10:00 - 10:15am	**Coffee Break**
10:15 - 11:30am	**Session 6: Special Session on ATPG and Compression,** Session Chair: TBD
	6.1 Automated Synthesis and At-Speed Test Generation Using On-Product Clock Generation Logic. Brion Keller*, Krishna Chakravadhanula, Tom Snethen (Cadence), Vikram Iyengar, David, Lackey and Gary Grise (IBM) 6.2 Achieving Desired Scan Compression. Brian Foutz*, Vijay Premchandar, Krishna Chakravadhanula, Brion Keller, Vivek Chickermane (Cadence) and Mary Kusko (IBM) 6.3 Analyzing Complex Test Initialization Sequences. Bryan Robbins, Scott Gaskins (Cadence), Mary Kusko* (IBM), James Allen and Mary Lou Ekstrom (Cadence)
11:30 - 12:30pm	**Lunch and Program Committee Meeting**
12:30 - 1:20pm	**Session 7: Wireless And Network Test,** Session Chair: TBD
	7.1 Building a DFM Team to Face the Test Challenges from Evolving Integrated Wireless Handset Devices. Tom Dean and Mark Bell (MediaTek Wireless) 7.2 Data Center Network Test Methodology And Application Performance Validation. Casimer DeCusatis (IBM)
1:20 - 3:05pm	**Session 8: Fault Models And DFT,** Session Chair: TBD
	8.1 Introduction to IEEE P1687/IJTAG. CJ Clark* (Intellitech) 8.2 Bridging Faults: A Case Study on Effectiveness In The Presence of Stuck-Fault And Transition Patterns With High Coverage. Kenneth Pichamuthu*, Kshitij Kulshreshta, Arun Raju and Vikram Iyengar (IBM) 8.3 Automated At-Speed Structural Test for ASICs. Pamela Gillis, Donald Hubbard, Vikram Iyengar* and Douglas Sprague (IBM)

** denotes presenter*