2009 IEEE NORTH ATLANTIC TEST WORKSHOP

MAY 13-15, LE CHAMBORD, HOPEWELL JUNCTION, NY 12533

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient testing methodologies and designs. With the increasing complexity in both design and test of integrated circuits and systems, the **18th NATW** features the theme: *"Simple Solutions Revolutionize Test"* and a **Panel** dedicated to Process Variation. This year NATW includes 30 papers from 7 different companies and 15 different universities, including 14 student papers competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes a **Special Session** dedicated to Solid State Circuits & Systems Test, and an **Invited Session** on Statistical Timing for Test of Process Variations. The 2009 workshop is held at Le Chambord in Hopewell Junction, NY, and is sponsored, in part, by the IEEE Green Mountain Section, the IEEE Circuits & Systems Society, and the IEEE Women in Engineering Committee. NATW corporate/academic supporters for 2009 include Mentor Graphics, SynTest Technologies, and Auburn University Wireless Engineering Research & Education Center.

Wednesday, May 13	
6:30 - 7:30pm	**Welcome Reception and Registration**
7:30 - 9:00pm	**Panel Session:** "Process Variation: The Line Blurs" Panel Chairs: Pascal Nsame and Gene Atwood (IBM) **Panelists**: Dean Adams (Aardvarkintellex), Yu Huang (Mentor), Bill Huott (IBM), Robert Smith (Verigy), Chandu Visweswariah (IBM)
Thursday, May 14	
7:00 - 8:00am	**Breakfast**
8:00 - 8:15am	**Opening Remarks:** Linda Milor (*General Chair*), Vikram Iyengar *(Program Chair)*
8:15 - 9:00am *Introduction by Vikram Iyengar, Program Chair*	**Keynote Address:** "Test and Characterization: Silicon Technology's Most Value-Add Step", Subu Iyer (IBM) **Abstract:** Technologists joke that test is what causes yield to plummet: Chips look great till we test them! However, over the last few years test has become a critical value-add step. The use of electrical fuses (eFUSEs), BIST, Built-in-self-repair (BISR), adaptive test circuits, testing of three dimensional interconnects and partially processed wafers, that may or may not be functional, is becoming more sophisticated and turning out to be a significant value add. We will give some examples of the impact this holistic approach to test has had.
9:00 - 9:45am *Introduction by Jennifer Dworak, Vice Program Chair*	**Invited Address:** "Scan Test Based Yield Learning", Wu-Tung Cheng (Mentor Graphics) **Abstract:** Nowadays, scan test failure diagnosis is commonly used to guide failure analysis to locate the root causes of yield problems. As technology nodes continue to scale, reaching mature yields becomes increasingly difficult. This presentation will first discuss the specific challenges in Yield Analysis and Failure Analysis that are resulting in slower yield ramps and lower mature yields. Secondly, a new approach to yield enhancement will be presented with silicon case studies. Lastly, we will discuss challenges in practical applications and future directions.
9:50 – 10:10am	**Coffee Break / Reception**
10:10 - 11:10am	**Student Session 1: Analog/Mixed-Signal Test,** Session Chair: Ted Cooley (Cooley & Co.)
	1.1 "Built-in Adaptive Test and Calibration of DAC", Wei Jiang* and Vishwani D. Agrawal (Auburn University) 1.2 "Polynomial Coefficient Based Multi-Tone Testing of Analog Circuits", Suraj Sindia*, Virendra Singh (Indian Institute of Science) and Vishwani Agrawal (Auburn University) 1.3 "Application of IDDq Testing to a Mixed-Signal Automotive IC with Combined Analog and Digital Power Domain", Andrew Laidler* and Jien-Chung Lo (University of Rhode Island)
11:10 - 11:50pm	**Student Session 2: Resistance and Fault Modeling,** Session Chair: Dean Adams (Aardvarkintellex)
	2.1 "Resistance Modeling for Noise Coupling in Lightly Doped Silicon Substrate", Charles Chiu* and Tian Xia (University of Vermont) 2.2 "Efficient Pattern Grading for Small Delay Defects in Digital Integrated Circuits", Ke Peng* (U. Conn), Mahmut Yilmaz, Krishnendu Chakrabarty (Duke U.), and Mohammad Tehranipoor (U. Conn)
12:00 - 1:00pm	**Lunch**
1:00 - 2:00pm	**Student Session 3: Test of Embedded Macros,** Session Chair: Yuejian Wu (Nortel)
	3.1 "Test-Wrapper Optimization for Embedded Cores in TSV-Based Three-Dimensional SOCs", Brandon Noia* and Krishnendu Chakrabarty (Duke University) 3.2 "Thermal Safe Modular Testing of Three-Dimensional System-on-Chip", Unni Chandran* and Danella Zhao (University of Louisiana at Lafayette) 3.3 "A Novel Fault Detection Architecture for Multiple Bit Upsets in Register Files", Wen Yueh* (Rutgers University) and Tapan J. Chakraborty (Alcatel-Lucent)

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Thursday, May 14	
2:00 - 3:00pm	**Student Session 4: Reliable and Secure Systems,** Session Chair: Pascal Nsame (IBM)
	4.1 “On Chip Via Wear Out Detection”, Fahad Ahmed* and Linda Milor (Georgia Tech.) 4.2 “Modeling Availability and Performability in High Performance Information Systems”, Syed Z. Shazli* and Mehdi B. Tahoori (Northeastern University) 4.3 “Security Threats and Defenses for JTAG”, Kurt Rosenfeld* and Ramesh Karri (Polytechnic Institute of NYU)
3:00 - 3:15pm	**Coffee Break**
3:15 - 4:15pm	**Student Session 5: BIST, DFT & Diagnosis,** Session Chair: Yu Huang (Mentor Graphics)
	5.1 “Built in Self Test Based on Delay Detection”, Fahad Ahmed* and Linda Milor (Georgia Tech.) 5.2 “DfT Toolbox - Something for Everybody”, Kemal Kulovic* and Martin Margala (U. Mass – Lowell) 5.3 “Compaction of Diagnostic Test Set for a Full-Response Dictionary”, Mohammed Ashfaq Shukoor* and Vishwani D. Agrawal (Auburn University)
4:45 pm	**Board bus to Social Program and Best Student Paper Award**
Friday, May 15	
7:30 - 8:00am	**Breakfast**
8:00 - 9:00am	**Session 6: Design-for-Test Innovations,** Session Chair: C.J. Clark (Intellitech)
	6.1 “H-Align: Improving the Scan Cell Observability of Horizontal Response Compactors”, Ozgur Sinanoglu* and Sobeeh Almukhaizim (Kuwait University) 6.2 “A Testable Scheme for Domino CMOS Circuits”, Vipin Sharma and Waleed K. Al-Assadi* (Missouri University of Science & Technology) 6.3 “A Green Solution to Random Testability”, Mary Kusko, Haoxing Ren, Rona Yaari and Victor Kravets* (IBM)
9:00 – 10:20am	**Session 7: Embedded Macro Test,** Session Chair: Jinjun Xiong (IBM)
	7.1 “Customized Algorithms for High Performance Memory Test in Advanced Technology Node”, Shomo Chen, Ning Huang (Trident Microsystems), Ting-Pu Tai* and Actel Niu (Mentor Graphics) 7.2 “A Case Study of Hierarchical Diagnosis for Core-Based SoC”, Eric Wang (Freescale), Yu Huang*, Wu-Tung Cheng, Wu Yang and James Fu (Mentor Graphics) 7.3 “Flexible and Powerful Test Method for Embedded Cores”, Bruce Cowan, Pam Gillis* and Kelly Ockunzzi (IBM) 7.4 “Built-In Functional Tests for Silicon Validation and System Integration of Telecom SoC Designs”, Yuejian Wu*, Sandy Thomson, Dale Mutcher and Eric Hall (Nortel)
10:20 - 10:30am	**Coffee Break**
10:30 - 11:30pm	**Session 8: Invited Special Session on Solid State Circuits & Systems Test,** Session Chair: Pascal Nsame (IBM)
	8.1 “Variability-Aware Methodology: The Crystal Ball for Smart Designs”, R. Joshi, R. Kanj and Y. Zhou (IBM) 8.2 “Design for Manufacturability Aware Placement, Routing and Cell Selection”, Shiyan Hu* (Michigan Tech.) 8.3 “Microelectronic Product Quality & Reliability: Design and Test Targeting Multiple Fabs”, Pascal Nsame (IBM)
11:30 - 1:00pm	**Lunch and Program Committee Meeting**
1:00 - 2:00pm	**Session 9: Advances in Delay Test,** Session Chair: Tapan J. Chakraborty (Alcatel-Lucent)
	9.1 “At-Speed Structural Test For Flexible-Scan Advanced-Nanometer Designs”, Vikram Iyengar*, Arun Raju, Gary Grise, Dave Lackey, Pam Gillis, Mike Ouellette, Frank Woytowich, Mark Taylor, Vineeta Shukla and Phil Stevens (IBM) 9.2 “Delay Defects, Coverage and Detection on the IBM S/390 zSeries 900 Microprocessor”, Mary Kusko*, Jim Crafts, Todd Cohen and Ulrich Baur (IBM) 9.3 “Speedpath Sourcing and Debug with Transition Fault ATPG on the Tukwila Processor”, Steve Yurash, Joshua Zelman*, Pankaj Pant and Rob Etter (Intel)
2:00 – 3:00pm	**Session 10: Invited Session on Statistical Timing for Test,** Session Chair: Mohammad Tehranipoor (U. Conn)
	10.1 “Test Generation for Process Variation Delay Defects”, Vladimir Zolotov*, Chandu Visweswariah and Jinjun Xiong (IBM) 10.2 “Statistical Ordering of Correlated Timing Quantities and its Application for Path Ranking”, Jinjun Xiong*, Chandu Visweswariah and Vladimir Zolotov (IBM) 10.3 “Statistical Multilayer Process Space Coverage for At-Speed Test”, Jinjun Xiong*, Yiyu Shi, Vladimir Zolotov and Chandu Visweswariah (IBM)

** denotes presenter*