2013 IEEE NORTH ATLANTIC TEST WORKSHOP

MAY 8-10, SHERATON COLONIAL BOSTON NORTH, WAKEFIELD, MA

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 22nd NATW will feature a general theme of "*Growing importance of Test and Hardware Security*."

This year's NATW includes 25 papers from 7 different companies and 8 different universities, including 12 student papers competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes a tutorial on "VLSI Test and Security", a Keynote Address on "**Testing Beyond the Specification: White Hat Engineers**" by Karen Panetta from Tufts University, a 1st Invited Address on "**How to Automate Analog DFT for ATPG**" by Stephen Sunter from Mentor Graphics, an IEEE Women in Engineering informational session, and a 2nd Keynote Address on "**Smarter Energy Trends, Challenges and Complexity: How do We Turn Data into Action?**" by Brian Gaucher from IBM. The 2013 workshop is being held at the Sheraton Colonial Boston North in Wakefield, MA and is sponsored, in part, by the Green Mountain and Boston sections of IEEE. It is organized in cooperation with TTTC and the IEEE Boston Section. NATW corporate and academic supporters for 2013 include Mentor Graphics, SynTest Technologies, Cadence, AdamsIP, Maxim, the Wireless Engineering Research and Education Center at Auburn University, IEEE Women in Engineering, and the Vermont chapter of the IEEE Solid State Circuits Society.

Wednesday, May 8

12:00 Registration

12:30-4:30 Invited Tutorial: "VLSI Test and Security"**,** Prof. Ramesh Karri (NYU-Poly) and Peilin Song (IBM T. J. Watson)

6:00 – 7:15pm Welcome Reception

7:30-9:00 pm Panel Session: "The Growing importance of Test and Hardware Security", Panel Moderator: Gene Atwood (IBM); Panel Chair: Yu Huang, Mentor Graphics; Panelists: Prof. Ramesh Karri (NYU-Poly), Peilin Song (IBM T. J. Watson), Prof. Mohammad Tehranipoor (Univ. of Connecticut), Prof. Jennifer Dworak (SMU).

Thursday, May 9

Registration

7:00 - 8:00 am Breakfast

8:00 - 8:15 am Opening Remarks: Paul Reuter, *General Chair*

8:15 - 9:00 am Keynote Address: "**Testing Beyond the Specification: White Hat Engineers**" by Karen Panetta, Tufts University

Introduction by Tian Xia, Program Chair

Abstract: For years, testing has been instrumental in the manufacturing of quality products to ensure that hardware and software perform to their specifications. Today, simulation and modeling tools dominate the design and test process and focus on detecting physical faults that can occur during the manufacturing process. However, given recent world events, engineers will have to learn to design and test to anticipate the abuses and re-purposing of their products for harmful intentions. These societal phenomena cannot currently be captured or anticipated in current simulations. This talk will discuss recent designs, design failures and the exploitation of technology for harmful purposes. Finally, we will discuss the new skills and tools needed to ensure that the technology we produce is not only reliable according to its specification, but also anticipates conditions beyond its specification.

9:00 - 9:45 am Invited Address: "**How to Automate Analog DFT for ATPG**" by Stephen Sunter, Mentor Graphics

Introduction by Tian Xia, Program Chair

Abstract: Analog design-for-test (DFT) lags digital DFT, and the costs of this are becoming clearer and less acceptable in industry (but not yet unacceptable). This presentation will show how much it is lagging, the reasons, how much it matters, and a strategy to catch up. History shows that no single company can eliminate this lag, so a concerted effort is needed to evolve an analog solution as successful as scan-based digital DFT has been for automatic test pattern generation (ATPG).

9:45 - 10:00 am Coffee Break / Reception

10:00 - 11:00 am Student Session 1: Advances in DFT & Low Power Test

Session Chair: Brion Keller - Cadence

10:00 - 10:20am *Ujjwal Guin (UConn, US)*: Novel DFTs for Circuit Initialization to Reduce Functional Fmax Test Time
10:20 - 10:40am *V. Sheshadri (AuburnU, US)*: Session-Less SoC Test Scheduling With Frequency Scaling
10:40 - 11:00am *P. Venkataramani (AuburnU, US)*: Test Programming for Power Constrained Devices

11:00 - 11:10 am Break

11:10 - 11:50 am Student Session 2: VLSI Test Security

Session Chair: Peilin Song- IBM

11:10 - 11:30am *Adam Zygmontowicz (SMU, US)*: Securing Test Hardware with Locking SIBs to Hide Instruments using P1687
11:30 - 11:50am *Ujjwal Guin (UConn, US)*: On Selection of Counterfeit IC Detection Methods

11:50 - 12:00 pm Break

12:00 - 1:00 pm Lunch

1:00 - 2:00 pm Student Session 3: Improving Yield & Reliability
Session Chair: Yong-Bin Kim- Northeastern University

1:00 - 1:20pm *C. Alagappan (AuburnU, US)*: Dictionary-Less Defect Diagnosis As Surrogate Single Stuck-At Faults
1:20 - 1:40pm *B. Zhang (AuburnU, US)*: Wafer Cut and Rotation for Compound Yield Improvement in 3D Wafer-on-Wafer Stacking
1:40 - 2:00pm *Qihang Shi (UConn, US)*: Experimental Analysis of Variations' Impact on Integrated Circuits

2:00 – 2:10 pm Break

2:10 - 3:30 pm Student Session 4: Analog and Mixed-Signal Test
Session Chair: Marvin Onabajo- Northeastern University

2:10 - 2:30pm *Hari Chauhan (NortheasternU, US)*: On-Chip Amplifier Linearity Calibration with the Fast Fourier Transform
2:30 - 2:50pm *J.P. Feng (NortheasternU, US)*: A Wide Dynamic Range Temperature Sensor for on-chip power monitoring
2:50 - 3:10pm *Rohit Shetty (UVermont, US)*: Low Cost Time Efficient OFDM Technique for Multitone Signal Generation
3:10 - 3:30pm *In-Seok Jung (NortheasternU, US)*: Test Methodology using Parametric Measurement Unit for ATE with 600 MHz DCL

3:30 - 3:45 pm Break

3:45 - 4:45 pm Paper Session: Reducing Test Cost
Session Chair: Yu Huang- Mentor Graphics

3:45 - 4:05pm *Ramesh Tekumalla (LSI Corp., US)*: Low Power Flip-flop design for reducing power consumption
4:05 - 4:25pm *Carl Wisnesky (Cadence, US)*: Very Low Pin Count Test Targeting A/D and Automotive Designs

4:25 - 6 pm Break

6 pm - 9 pm Banquet and Best Student Paper Award (Location: Hawthorne Hotel, Salem, MA)

Friday, May 10

7:30 – 2:00pm Registration

7:30 - 8:00 am Breakfast

8:00 - 8:45 am Friday Keynote Address: "Smarter Energy Trends, Challenges and Complexity: How do We Turn Data into Action?" by Brian Gaucher, IBM

Abstract: Worldwide energy use is growing rapidly, reliability is suffering and supplies are currently being stretched to point of breaking. As we look across the energy domain, there are at least five complex areas of energy experiencing major challenges. We are at an interesting inflection point of smart grid and the IT revolutions, that we will explore to see what solutions might be available to address these. In so doing, we will come to the question of, "Can the coming age of Cognitive systems and related technologies be applied to transform the peta to exa bytes of real-time and historical data, into actionable decisions to address these challenges?"

8:45 - 8:55 am Break

8:55 - 10:15 am Paper Session: Hierarchical Test for SoCs & 3D Packages
Session Chair: Vishwani Agrawal- Auburn University

8:55 - 9:15am *Ramesh Tekumalla (LSI Corp., US)*: Interconnect Fault Testing between cores using efficient wrapper cells
9:15 - 9:35am *Brion Keller (Cadence, US)*: Efficient Testing of Hierarchical Core-Based SOCs
9:35 - 9:55am *Yu Huang (Mentor Graphics, US)*: Test Access Mechanism for TSV Characterization in 3D ICs
9:55 - 10:15am *Krishna Chakravadhanula (Cadence, US)*: ASIC Embedded Macro Test in an IEEE P1687 Environment

10:15 - 10:30 am Break

10:30 - 11:50 am Paper Session: Industrial Test Practices
Session Chair: Bradley D Pepper – IBM

10:30 - 10:50am *Ramesh Tekumalla (LSI Corp., US)*: At-Speed Scan Test of Memory Functional Interface
10:50 - 11:10am *Yu Huang (Mentor Graphics, US)*: Diagnosis and Layout Aware (DLA) Scan Chain Stitching
11:10 - 11:30am *Peter Sarson (AMS AG, Austria)*: Automotive EEPROM qualification and cost optimization
11:30 - 11:50am *Ramesh Tekumalla (LSI Corp., US)*: Clock Domain based Scan Enable Separation for Enhanced Delay Fault Coverage

11:50 - 12:00 pm Break

12:00 - 1:00 pm Lunch and Program Committee Meeting

1:00 - 2:00 pm IEEE Women in Engineering Session
Session Chair Denise Griffin, WIE Boston Chair

1:00 - 1:30pm *Denise Griffin (WIE Boston Chair)*: What is IEEE WIE (Women in Engineering)?
1:30 - 1:50pm *Iris Bahar (Brown Univ., US)*: Harnessing an FPGA for Built-in Self-Repair in a 3D Die Stack

1:50 - 2:00 pm Break

2:00 - 2:40 pm IBM Special Session
Session Chair: Pascal Nsame - IBM

2:00 - 2:20pm *Bradley Pepper (IBM, US)*: Using Adaptive Test Pattern Sampling to Test Integrated Circuits
2:20 - 2:50pm *Mustapha Slamani (IBM, US)*: The Rapid Evolution of Wireless Products: The Challenges behind RF and Millimeter-Wave Design, Test, and High-Volume Manufacturing

2:50-3:00 pm Closing Remarks, Paul Reuter