2014 IEEE NORTH ATLANTIC TEST WORKSHOP

MAY 14-16, TRADITIONS AT THE GLENN, JOHNSON CITY, NY

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 23nd NATW will feature a general theme of "*Growing Need for Standards in Test Hardware and Methodologies*."

This year's NATW includes 27 papers from 8 different companies and 12 different universities, including 17 student papers competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes a tutorial on "*Core Based SoC Hierarchical Test: The Methodologies and Industry Practice*", a Keynote Address on "**Silicon Authentication Platform**" by Prof. Mark (Mohammad) Tehranipoor from University of Connecticut, a 1st Invited Address on "**CloudTesting™ Service, a revolutionary concept for Post-silicon validation**" by Mani Balaraman from Advantest, and a 2nd Keynote Address on "**Overview of System-On-Chip for Military Applications**" by Tommy Lam from Lockheed Martin. The 2014 workshop is being held at the Traditions at the Glenn Resort and Conference Center, Johnson City, NY and is sponsored by the IEEE Binghamton Section in cooperation with the IEEE Green Mountain Section. NATW corporate and academic supporters for 2014 include Cadence, Mentor Graphics, SynTest Technologies, AdamsIP, Maxim and Advantest.

Wednesday, May 14	
12:00 pm	**Registration**
1:00 - 4:30 pm	**Invited Tutorial:** "Core Based SoC Hierarchical Test: The Methodologies and Industry Practice", Presenters: Brion Keller (Cadence Design Systems) and Yu Huang (Mentor Graphics)
4:30 - 5:00 pm	**Break**
5:00 - 7:00 pm	**Visit Endicott History and Heritage Center** (Featuring the history of Endicott, NY - Birthplace of IBM)
7:00 - 8:00 pm	**Welcome Reception**
8:00 - 9:30 pm	**Panel Session:** "Does P1687 bring something to the table that is not satisfied by 1838, 1500 and 1149.1?", Panel Moderator: Gene Atwood (IBM); Panel Chair: Yu Huang, Mentor Graphics; Panelists: CJ Clark (Intellitech), J-F. Cote (Mentor Graphics), Vivek Chickermane (Cadence), Sudipta Bhawmik (Qualcomm)
Thursday, May 15	
7:00 - 5:00 pm	**Registration**
7:00 - 8:00 am	**Breakfast**
8:00 - 8:10 am	**Opening Remarks:** Paul Reuter, *General Chair*
8:10 - 8:55 am *Introduction by Tian Xia, Program Chair*	**Keynote Address:** "**Silicon Authentication Platform**" by Prof. Mark (Mohammad) Tehranipoor, University of Connecticut **Abstract:** Design and fabrication of integrated circuits (ICs) have become increasingly vulnerable to malicious activities, security attacks, counterfeiting activities, and reliability with globalization and further scaling of technology. In this talk we will discuss some of these challenges that semiconductor and EDA industry have to deal with and present solutions to mitigate the threats.
8:55 - 9:40 am *Introduction by Tian Xia, Program Chair*	**Invited Address:** "**CloudTesting™ Service, a revolutionary concept for Post-silicon validation**" by Mani Balaraman, Advantest **Abstract:** The portable Cloud Testing Station is a revolutionary test services concept for semiconductor design verification, DFT, QA and RMA testing. A small form factor test station and on-demand down-loadable test IPs needed for the target applications provides a step function improvement in overall time to market and lowest investment needed. The users don't pay for the HW. The downloadable IPs are charged on a monthly basis dramatically cutting down users upfront investment and align with the usage model. GUI based user interface eliminates the need for learning programming language and HW making it easy for non-ATE users like design, DFT and QA engineers.
9:40 - 9:50 am	**Coffee Break / Reception**
9:50 - 10:50 am	**Student Session 1: Advances in Test Generation** **Session Chair:** Nur Touba, Univ. of Texas at Austin
9:50 - 10:10am 10:10 - 10:30am 10:30 - 10:50am	*Fanchen Zhang (SMU, US)*: When Optimized N-Detect Test Sets are Biased: An Investigation of Cell-Aware-Type Faults and N-Detect Stuck-At ATPG *M. Venkatasubramanian (AuburnU, US)*: New Test Vector Search Algorithm for a Single Stuck-at Fault using Probabilistic Correlation *Yukun Gao (Texas A&M, US)*: Delay Test of Embedded Memories
10:50 - 11:00 am	**Break**

11:00 - 12:00 pm	**Student Session 2: Innovations in Test Security & Biochips** **Session Chair:** Sudipta Bhawmik, Qualcomm
11:00 - 11:20am	*Md. Tauhidur Rahman (UConn, US)*: CSST: An Efficient Secure Split-Test for Preventing IC Piracy
11:20 - 11:40am	*Yu-Wei Lee (UT Austin, US)*: Improving Logic Obfuscation via Logic Cone Analysis
11:40 - 12:00pm	*Kai Hu (DukeU, US)*: Testing of Flow-Based Microfluidic Biochips and Experimental Demonstration
12:00 - 1:00 pm	**Lunch**
1:00 - 2:00 pm	**Student Session 3: Reducing Test Cost** **Session Chair:** Ted Cooley, Cooley & Company
1:00 - 1:20pm	*Gustavo K. Contreras (UConn, US)*: TAME-TPI: A Timing-Aware Metric for Efficient Test Point Insertion and Area Overhead Reduction
1:20 - 1:40pm	*Baohu Li (AuburnU, US)*: Testing With Reduced ATE Channels
1:40 - 2:00pm	*Konstantin Shibin (TallinnU, Estonia)*: Asynchronous fault detection in IEEE P1687 instrument network
2:00 - 2:10 pm	**Break**
2:10 - 3:30 pm	**Student Session 4: Analog and Mixed-Signal Test** **Session Chair:** Pascal Nsame, Polytechnique Montreal
2:10 - 2:30pm	*M. Metwally (UVermont, US)*: Compressive Sampling Coupled OFDM Technique for Testing Continuous Wave Radar
2:30 - 2:50pm	*Dong An (McGillU, US)*: Design of a Programmable SoC Test System
2:50 - 3:10pm	*Yujia Peng (USouthCarolina/Virginia CommonwealthU, US)*: Characterization of a Passive Telemetric System for ISM Band Pressure Sensors
3:10 - 3:30pm	*Yujia Peng (USouthCarolina/UVermont, US)*: On-Wafer Calibration Technique for High Frequency Measurement with Simultaneous Voltage and Current Tuning
3:30 - 3:45 pm	**Break**
3:45 - 4:45 pm	**Student Session 5: Power-Aware Test** **Session Chair:** Themistoklis Haniotakis, Southern Illinois University
3:45 - 4:05pm	*Sindhu Gunasekar (AuburnU, US)*: Optimal Selection of ATE Frequencies for Test Time Reduction Using Aperiodic Clock
4:05 - 4:25pm	*Tengteng Zhang (Texas A&M, US)*: Pattern Generation for Post-Silicon Timing Validation Considering Power Supply Noise
4:25 - 4:45pm	*Aymen Touati (LIRMM-UM2/CNRS, France)*: A Comprehensive Evaluation of Functional Programs for Power-Aware Test
4:45 - 5:30 pm	**Break**
5:30 - 10:00 pm	**Social Event: Banquet and Best Student Paper Award** (Location: Greek Key, Endicott, NY) **Broadway-style show "Sirens" at the Cider Mill Playhouse** (Endicott, NY)
Friday, May 16	
7:30 - 2:00 pm	**Registration**
7:30 - 8:00 am	**Breakfast**
8:00 - 8:45 am *Introduction by Tian Xia, Program Chair*	**Friday Keynote Address:** "**Overview of System-On-Chip for Military Applications**" by Tommy Lam, Fellow, Lockheed Martin **Abstract:** We are in the System-On-Chip (SoC) revolution age where electronics devices can maturely be realized with orders of magnitude better Size, Weight, And Power and Cost (SWaP-C) than when the electronic industry first started 4 decades ago. This SoC revolution fundamentally benefits a wide range of technologies in both the commercial and defense sectors. This keynote speech will provide an overview of essential SoC technologies for Military applications such as Radio Frequency Field Programmable Gate Array (RF-FPGA); Digital Radio SoC, Advanced Electronic Warefare (EW), Unmanned Aerial Systems (UAS), and Supply Chain Hardware Integrity for Electronics Defense (SHIELD).
8:45 - 9:30 am *Introduction by Tian Xia, Program Chair*	**Invited Address:** "" by Prof. Amit Lal, Cornell University **Abstract:** TBD
9:30 - 9:45 am	**Coffee Break**
9:45 - 10:45 am	**Paper Session 1: Industrial Best Practices**

Session Chair: Tommy Lam, Lockheed Martin

9:45 - 10:05am *Ramesh Tekumalla (LSI Corp., US)*: On-Chip Clock Testing and Frequency Measurement
10:05 - 10:25am *Leon Palmer (IBM/Cadence, US)*: Highly Effective and Scalable Distributed ATPG Architecture and Application to a Commercial ASIC
10:25 - 10:45am *Yu Huang (Mentor Graphics, US)*: Identify Faulty Scan Chains for Multiple Fanout Space Compactors

10:45 - 10:55 am Break

10:55 - 11:55 am Paper Session 2: Beyond the Digital Frontier
Session Chair: Brion Keller, Cadence

10:55 - 11:15am *Pascal Nsame (Polytechnique Montreal, Canada)*: Design and Test of Adaptive Computing Fabrics For Scalable and High-Efficiency Cognitive SoC Applications
11:15 - 11:35am *Tommy Lam (Lockheed Martin, US)*: Innovative Antenna Chamber Characterization
11:35 - 11:55am *Grace Tang (IEEE Binghamton, US)*: Power System Fault Modeling/Simulation Protective Relay Testing and Simulation

11:55 - 12:00 pm Break

12:00 - 1:00 pm Lunch and Program Committee Meeting

1:00 - 2:00 pm Paper Session 3: Memory Test
Session Chair: Yu Huang, Mentor Graphics

1:00 - 1:20pm *Ramesh Tekumalla (LSI Corp., US)*: Local Repair Signature Handling for Repairable Memories
1:20 - 1:40pm *Kelly Ockunzzi (IBM/SiVision, US)*: Optimizing Delay Tests at the Memory Boundary
1:40 - 2:00pm *Ramesh Tekumalla (LSI Corp., US)*: On Handling Memory Scan Chains

2:00 - 2:10 pm Break

2:10 - 2:50 pm Paper Session 4: Hierarchical Test for SoCs & 3D Packages
Session Chair: Sudipta Bhawmik, Qualcomm

2:10 - 2:30pm *Christos Papameletis (IMEC/Cadence, Netherlands/US)*: A 3D-DfT Demonstrator Test Chip
2:30 - 2:50pm *Yu Huang (Mentor Graphics, US)*: Test Compression Improvement with EDT Channel Sharing in SoC Designs

2:50-3:00 pm Closing Remarks, Paul Reuter

** denotes presenter*