

2016 IEEE NORTH ATLANTIC TEST WORKSHOP
MAY 9-11, CROWNE PLAZA HOTEL PROVIDENCE-WARWICK, RHODE ISLAND

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 25th NATW features a general theme of “Celebrating 25 Years of NATW”.

This year’s NATW includes 18 peer reviewed research papers co-authored by researchers from 6 companies and 9 universities, including 12 student papers, which are competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes an embedded tutorial by Erik Larsson from Lund University, two Keynote Addresses by John Carulli from GlobalFoundries and Shawn Blanton from Carnegie Mellon University, and two Invited Talks from Yang Liu from IBM and Derryl Allman from ON Semiconductor. The 2016 workshop is being held at the Crowne Plaza Hotel Providence-Warwick, Rhode Island, and is sponsored by the IEEE Providence Section in cooperation with the IEEE Green Mountain Section.

Monday, May 9

12:00 - 5:00 pm Registration

12:00 - 1:00 pm Lunch

1:00 - 2:30 pm Tutorial: “Accessing embedded instruments using IEEE 1687”
Erik Larsson, Lund University, Sweden

Abstract: The electronic systems we find in almost every product today are implemented using integrated circuits (ICs) mounted on printed circuit boards (PCBs). Developing electronic systems is a challenging task due to complexity and miniaturization. Design-for-Test (DfT) features, so called instruments, are embedded on-chip in modern ICs to handle and monitor various activities. Many defects are handled at IC manufacturing; however, there are many problems occurring after ICs are being mounted on PCBs. In many cases, it is not possible to reproduce the problem when the electronic system is taken to a repair shop. One obstacle is the limited access to the on-chip DfT instruments that exist in most ICs. We will discuss access to on-chip DfT instruments through the life-time of electronic systems. We will focus on electronic systems using the IEEE 1687 standard.

2:30 - 2:40 pm Coffee Break

2:40 - 2:50 pm Opening Remarks: Brion Keller, *General Chair*

2:50 - 3:40 pm Keynote Address: “What is a failure? Why should I care?”
John Carulli, GlobalFoundries, US

Introduction by Brion Keller, General Chair
Abstract: For advanced CMOS technologies, we are now capable of creating billions to trillions of transistors per design. Following the economic path of Moore's law, we have built expertise as we went sub-lithography to fool light. We have integrated new materials at an increasing pace to drive performance, power, and reliability. We are integrating vertically with 2.5D/3D packaging and starting monolithic 3D. These advances brought and are continuing to bring significant challenges in dealing with variation. Designers have been managing variation by using adaptive circuit and system approaches. Essentially changing the design to accommodate the distribution. What is the impact to Test following traditional functional, structural, and spec-based testing approaches?

3:40 - 5:00 pm Student Session 1: Analog and RF

Session Chair: *J.C. Lo (Univ. of Rhode Island, US)*

- 3:40 - 4:00 pm *Gyunam Jeon (Northeastern Univ, US): A 100MS/s 10-bit Split-SAR ADC with Capacitor Mismatch Compensation Using Built-In Calibration*
- 4:00 - 4:20 pm *Gyunam Jeon (Northeastern Univ, US): An Area Effective 4Gb/s Half-Rate 3-Tap DFE with Current-Integrating Summer for Data Correction*
- 4:20 - 4:40 pm *Jiafei Yao (UVermont, US): Case Study: A 27 GHz LNA Circuit Diagnosis and Layout Modification with Electromagnetic Simulations*
- 4:40 - 5:00 pm *Marvin Onabajo (Northeastern Univ, US): A Tuning Technique for Temperature and Process Variation Compensation of Power Amplifiers with Digital Predistortion*

5:00 - 6:00 pm Break

6:00 - 7:30 pm Welcome Reception

7:30 - 9:00 pm Panel Session: “Visions of The Internet of Things”

Panel Chair: *Gene Atwood (IBM, US)* **Moderator:** *Malinky Ghosh (GlobalFoundries, US)*

Panelists: *Kunal Mankodiya (University of Rhode Island, US), John Carulli (GlobalFoundries, US), Erik Larsson (Lund University, Sweden), Pascal Nsame (Kardinal Microsystems, US), Derryl Allman (ON Semiconductor, US)*

2016 IEEE NORTH ATLANTIC TEST WORKSHOP
MAY 9-11, CROWNE PLAZA HOTEL PROVIDENCE-WARWICK, RHODE ISLAND

Tuesday, May 10

7:30 - 12:00 pm Registration

7:30 - 8:20 am Breakfast

8:20 - 9:00 am Invited Address: "Potential paradigm shift for 3D fine-pitch test"
Yang Liu, IBM TJ Watson Research Center, US

Introduction by Program Chair **Abstract:** TSV-based 3D silicon technology has been emerging in commercial products. No matter what integration Nicola Nicolici scheme is chosen, test and cumulative yield are critical. Fine pitch probing is difficult with traditional probe card technologies. It is important to achieve good coplanarity, high probe accuracy, low probing force, low bump damage, low parasitics, high current capability, high test speed, etc., in a cost-effective manner. Even with a successful probing method, good chips can still be wasted in a bad stack if a defective layer could not be removed or repaired. Last but not least, a 3D test flow may require a number of test insertions, which could be costly and/or impractical, although simplified test flow could be adopted in special cases.

9:00 - 10:20 am Student Session 2: Modeling, Diagnosis and Debug
Session Chair: *Paul Reuter (Mentor Graphics, US)*

9:00 - 09:20 am *Md Nazmul Islam (UMass Amherst, US):* Modeling Residual Life of an IC considering Multiple Aging Mechanisms
 9:20 - 09:40 am *Abhishek Koneru (Duke Univ, US):* Analysis of Electrostatic Coupling in Monolithic 3D Integrated Circuits and its Impact on Delay Testing
 9:40 - 10:00 am *Kamran Saleem (UT Austin, US):* Improving Diagnosis from Compacted Response Using Symbolic Canceling
 10:00 - 10:20 am *Andrey Tolstikhin (McGill Univ, Canada):* Enabling Debug in IoT Wireless Development and Deployment With Security Considerations

10:20 - 10:40 am Coffee Break

10:40 - 12:00 pm Student Session 3: Advances in Test Generation and Application
Session Chair: *Andrew Laidler (ON Semiconductor, US)*

10:40 - 11:00 am *Muralidharan Venkatasubramanian (Auburn U, US):* Failures Guide Probabilistic Search for a Hard-to-Find Test
 11:00 - 11:20 am *Yi Sun (SMU, US):* Using Existing Reconfigurable Logic in 3D Die Stacks for Test
 11:20 - 11:40 am *Fanchen Zhang (SMU, US):* Harnessing Scan Shift Cycles for Probabilistic Fault Detection
 11:40 - 12:00 pm *Joseph Nguyen (STMicroelectronics and IMEP-LAHC, France):* RAPIDO Testing and Modeling of Assisted Write and Read Operations for SRAMs

12:00 - 1:00 pm Lunch

1:00 - 6:00 pm Social Event: Field trip to visit the Breakers Mansion in Newport County
<http://www.newportmansions.org/>

6:00 - 7:00 pm Break

7:00 - 9:00 pm Social Event: Banquet at Crowne Plaza Hotel including

- The announcements of the **Jake Karrfalt Best Student Paper Award**
Excellence in Design and Test Engineering Award
James Monzel Service Award
- A talk from the NATW steering committee co-chairs Xinghao Chen and Ted Cooley on
Celebrating 25 Years of NATW

2016 IEEE NORTH ATLANTIC TEST WORKSHOP
MAY 9-11, CROWNE PLAZA HOTEL PROVIDENCE-WARWICK, RHODE ISLAND

Wednesday, May 11

7:30 - 12:00 pm Registration

7:30 - 8:10 am Breakfast

8:10 - 9:00 am Keynote Address: “Design, test and diagnosis of logic characterization vehicles”
Shawn Blanton, Carnegie Mellon University, US

Introduction by Program Chair **Abstract:** A new semiconductor fabrication technology always has unknown detriments that need to be discovered and remedied through the fabrication and analysis of test structures and test chips. Passive structures such as combs, serpentines, and via arrays are fairly straightforward in that they both capture low-level characteristics of real designs and are transparent to failure. That is, when failure occurs, it is straightforward to both precisely localize the failure and characterize its root cause. The same is generally true for some active test circuits such as ring oscillators and memories. Unfortunately, this is not the case for the logic characterization vehicle (LCV). An LCV is a test chip composed of standard cells that are fabricated to validate a new library in a new technology. Conventional LCVs are either a product-like sub-circuit, or a probe- or scan-based sea of isolated gates, where the former inherently reflects actual characteristics of real designs, and the latter has excellent testability and diagnosability. In this talk, I will describe our work in the Advanced Test Chip Laboratory (www.ece.cmu.edu/~actl) to develop a design, test, and diagnosis methodology for an LCV that is both highly reflective of actual designs and ultra-testable and diagnosable.

9:00 - 9:40 am Invited Address: “IoT: The real story”
Derryl Allman, ON Semiconductor, US

Introduction by General Chair **Abstract:** There have many published reports on the Internet of Things (IoT) describing a wide range of market sector growth opportunities. The rate of growth is dependent on current and future internet infrastructure, value added, number of users, and cost pressures. The complexity of interconnect connectivity, data sharing and concerns over security will determine the IoT revenue stream, job and business opportunities. Currently, we are on the edge of IoT system integration and subsequent increase in device proliferation. The progressive increase in demand and cost reduction will challenge design flexibility and impact test methods for scalability and functional test coverage.

9:40 - 10:20 am Industry Session 1: ASIC and Microprocessor Test
Session Chair: *Vishwani Agrawal (Auburn University)*

9:40 - 10:00 am *Malinky Ghosh (GlobalFoundries, US):* Automated and Reusable IP Functional Test Rule Development across multiple IP Instances within and across ASIC designs
 10:00 - 10:20 am *Brion Keller (Cadence, US):* Using IBM Power 8 to Develop a Hierarchical Test Methodology

10:20 - 10:40 am Coffee Break

10:40 - 12:00 pm Industry Session 2: Compression, BIST and Root Cause Identification
Session Chair: *Iris Bahar (Brown University)*

10:40 - 11:00 am *James Fu (Mentor Graphics, US):* Case Study of Testing a SoC Design with Mixed EDT™ Channel Sharing and Channel Broadcasting
 11:00 - 11:20 am *Paul Logsdon (IBM, US):* Integrated Scan Diagnostic Technique using Laser Stimulation and LBIST
 11:20 - 11:40 am *Pascal Nsame (Kardinal Microsystems, US):* Autonomous BIST Architecture for 5G and IoT Applications
 11:40 - 12:00 pm *Kannan Sekar (GlobalFoundries, US):* Accelerating Root Cause Identification by Integrating All Data Types

12:00 - 1:00 pm Closing remarks and Lunch