2018 IEEE North Atlantic Test Workshop

May 7-9, 2018, Essex Resort & Spa, Essex, Vermont

The IEEE North Atlantic Test Workshop (NATW) provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 27th NATW features a general theme of "Silicon Photonics." The 2018 workshop is being held at the Essex Resort & Spa, Essex, Vermont, and is sponsored by IEEE-USA, IEEE Region 1 and IEEE Green Mountain Section.

Monday, May 7
10:00 am – 4:30 pm Registration
10:50 am – 11:00 am Welcome Address
11:00 am – 4:30 pm Seminars
• 11:00 am – 12:00 pm Seminar 1: John Ferrario & Fen Guan (GF): Photonics Test Systems for Modeling, Process Monitoring and Final Test.
12:00 pm – 1:00 pm Lunch
• 1:00 pm – 2:00 pm Seminar 2: Thomas Brown (AIM Photonics): The status, needs and potential solutions related to testing photonic devices and products including those that Incorporate Photonic Integrated Circuits (PIC)
2:00 pm – 2:15 pm Break
• 2:15 pm – 3:15 pm Seminar 3: Mustapha Slamani (GF): Enabling Cost-Effective 5G Phased Array mmWave Testing
3:15 pm – 3:30 pm Coffee Break
• 3:30 pm – 4:30 pm Seminar 4: Dean Adams (IP/Patent): Patenting & Entrepreneurship for the Test Industry
6:00 pm Dinner
7:00 pm – 9:00 pm Panel Discussions – Juan Sanchez (OnSemi), Thomas Brown (AIM Photonics), Bryan McDonald (GF), Hanyi Ding (GF), Michael Shur (RPI), Eugene Atwood (IBM), "Silicon Photonics."
Tuesday, May 8
7:30 am – 12:00 pm Registration
7:30 am – 8:20 am Breakfast
8:20 am – 8:30 am Welcome Address
8:30 am– 9:25 am Keynote Address 1: John Ferrario & Fen Guan (GF): Photonics Test Systems for Modeling, Process Monitoring and Final Test.
9:25 am – 9:35 am Coffee Break
9:35 am – 10:30 am Invited Address 1: Sule Ozev (ASU): BIST for LDOs Using Pseudo-Random Excitation and Cross-Correlation
10:30 am – 12:00 pm Academia Session 1 **Chair:** Kenneth Butler
• 10:40 am – 11:00 am Anurag Tulsiram, William R. Eisenstadt (U. Florida): Development of LDO Testing and Fault Detection for Ultra Low Defects.
• 11:00 am – 11:20 am Mehmet Ince (Arizona State Univ.), Ender Yilmaz (NXP), and Sule Ozev (Arizona State Univ.) Enabling Fast Process Variation and Fault Simulation Through Macromodelling of Analog Components.
• 11:20 am – 11:40 am Hui Jiang, Jennifer Dworak (SMU), One More Time! Increasing Fault Detections with Scan Shift Capture.

- 11:40 am – 12:00 pm Wei Jiang, Guoan Wang (Univ. South Carolina): A simplified on-chip calibration method for branch-line coupler

12:00 pm – 1:00 pm Lunch

1:00 pm – 2:00 pm Academia Session 2 **Chair:** Kelly Ockunzzi

- 1:00 pm – 1:20 pm Timothy M. Platt, Chen Liu (Clarkson Univ.), Reducing Test Time with FPGA Accelerators Using OpenCL.
- 1:20 pm – 1:40 pm Michael Shur & John Suzrez (Rensselaer Polytechnic Institute): Nanoscale Silicon MOSFET Response to THz Radiation for Testing VLSI.
- 1:40 pm – 2:00 pm Weize Yu and Yiming Wen (Old Dominion Univ.): A Novel Strong PUF Architecture Based on On-Chip Voltage Regulation

2:00 pm – 2:10 pm Break

2:10 pm – 2:40 pm Invited Address 2: David Yeh (SRC): Trends Driving SRC Test Research Funding

2:40 pm – 2:50 pm Coffee Break

2:50 pm – 3:50 pm Invited Address 3: Juan Pulido Sanchez (On Semiconductor): DFT solutions for High Speed Interfaces in Image Sensors

3:50 pm – 4:00 pm Break

4:00 pm – 5:30 pm Industry Session 1 **Chair:** Danella Zhao

- 4:00 pm – 4:30 pm Kelly Ockunzzi, Richard Grupp(GF): Our Experience with Hierarchical Test
- 4:30 pm – 5:00 pm Brion Keller (GF): Automating Patterns to the Tester
- 5:00 pm – 5:30 pm Rajesh Khurana (Cadence): Evolution of IEEE 1687 – Past, Present and the Future

5:30 pm – 6:00pm Break

6:00 pm – 8:30 pm Social Event: Banquet : a cappella group performing – "Root 7"

Wednesday, May 9

7:30 am – 12:00 pm Registration

7:30 am – 8:10 am Breakfast

8:10 am – 9:10 am Keynote Address 2: Yiorgos Makris (UT Dallas), Applications of Machine Learning in Semiconductor Manufacturing and Test.

9:10 am – 10:40 am Industry Session 2 **Chair:** Weize Yu

- 9:10 am – 9:40 am Ryan Pennucci, Ryan Jurasek, Wolfgang Hokenmaier, Lester Patrick, Jacob Bucci, Donald Labrecque, David Kinney (Green Mountain Semiconductor), An Analysis of Inexpensive Memory Test Solution.
- 9:40 am – 10:10 am Nabil El Belghiti Alaoui, Patrick Tounsi, Alexandre Boyer (Laboratory LAAS-CNRS), Armaud Viard (ACTIA Automotive), New testing approach using near electromagnetic field probing intending to upgrade in-circuit testing of high density PCBAs.
- 10:10 – 10:40 am Andrew Laidler (On Semi): Next-generation ATE (Automated Test Equipment) Case Study of Automotive Mixed-Signal Semiconductor Testing

10:40 am – 10:50 am Coffee Break

10:50 am – 11:50 am Industry Session 3 **Chair:** John Potter

- 10:50 am – 11:20 am Krishna Mohan Chavali, SMTS, REL-ENG (Global Foundries), Wafer Level High Temperature Test Scheme for Quick Functional and Reliability Assessments.
- 11:20 am – 11:50 am Imtiaz Ahmed, Subhash Baraiya (Qualcomm), Rahul Singhal (Mentor), Case Study on Low Pin Count Testing of Industry Transceiver Chip.

11:50 am – 12:00 pm Closing Remarks

12:00 pm – 1:00 pm Lunch