North Atlantic Test Workshop 2020

The IEEE North Atlantic Test Workshop (NATW) provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 29th NATW features a general theme of "Achieving Semiconductor Reliability: Without Burn-In." To support education of our attendees and enable a common vocabulary for the panel discussion theme, the first sessions tutorial will provide a broad perspective on reliability, from Systems, packaging to integrated semiconductors.

The North Atlantic Test Workshop (NATW) 2020 will be held as two subsequent Wednesday morning sessions using Zoom webinar. Advance registration and a nominal fee are required to register for the two session event.

– Pandemic *Virtual* Edition Theme - ***"Achieving Semiconductor Reliability: Without Burn-In."***

June 17, 10AM to 1PM EST Paper Session
June 24, 10AM to 1PM EST Tutorial and Panel

Please learn more about the IEEE sponsored North Atlantic Test Workshop and how to register at natw.ieee.org. Event pricing includes post workshop access to presented papers and tutorial presentation content. After paying using the Paypal* payment portal, please complete your registration by filling out the registration form.

*accepts credit card transactions without becoming a Paypal member

NATW-2020 is sponsored by IEEE Schenectady Section and IEEE Region 1, and is supported by IBM Corp., Advantest America, AdamsIP, Mentor (A Siemens Business), Cadence Design Systems, Green Mountain Semiconductor and On Semiconductor.

IEEE Member:	$40
IEEE Life Member:	$20
IEEE Member, Student:	$20
Non-IEEE Member:	$50
Non-IEEE Member, Student:	$25

The full agenda is included here:

Wednesday, June 17 **(Presentation minutes are tentative and will be finalized close to but before June 17.)**
10:00 am – 10:05 am Introduction and Welcome: Eugene Atwood General Chair
10:05 am – 10:10 am Introduction and Welcome: James Lloyd Program Chair
10:10 am – 10:40 am Invited Speaker: "Large-scale statistical analysis of early failures in Cu electromigration" Martin Gall With continuing scaling of Cu-based metallization, the electromigration failure risk has remained one of the most important reliability concerns for advanced process technologies. The main factors requiring attention are the activation energy related to the dominating diffusion mechanism, the current exponent as well as the median lifetimes and lognormal standard deviation values of experimentally acquired failure time distributions. In general, the origin and scaling behavior of these parameters are relatively well understood. However, the observation of bimodality in dual-inlaid Cu interconnects has added high complexity. Nanoscale electromigration-induced voids, requiring only a very limited amount of mass movement, can cause early failures and lead to severe concerns with respect to long-term, reliable chip operation at use conditions. For a more thorough investigation of these early failure phenomena, specific test structures were designed based on the Wheatstone Bridge technique. The use of these structures enabled an increase in the tested sample size past 800,000 for the 90 nm technology node, allowing a direct analysis of EM failure mechanisms at the single-digit

ppm regime for the first time. These studies were continued for the 65, 40, 28, and 12 nm technologies, encompassing a total sample size of more than 1.5 million until the present time. This talk will give an overview of the development of the Wheatstone Bridge technique for early failure detection and highlight the main physical findings pertaining to the understanding of electromigration-induced degradation phenomena in advanced interconnects.

Martin Gall is the director of the Reliability Engineering Department at Globalfoundries in Malta, NY. He started his work in semiconductor reliability at Motorola/Freescale in 1995 as an engineer, He has (co)authored more than 70 publications, and is an editor for the IEEE Transactions on Device and Materials Reliability.

Academic Contributions Format is 15 minutes and 5 minutes Q&A

10:40 am – 11:00 am Paper 1: "A Built In Test circuit for waveform classification at high frequencies" Konstantinos Poulos, Themistoklis Haniotakis

We introduce a new Build In Test (BIT) signature generator for functional verification and output classification of RF integrated circuits. The proposed circuit is a single rectifier based MOS transistor, with the substrate and gate independently biased to control source terminal voltage range, followed by a passive RC filter. In normal operation the proposed low cost test scheme ensures the minimum effect at the performance of the measured circuit under test

Presenting Author: Konstantinos Poulos, Southern Illinois University
The author is currently a PhD student at Southern Illinois University in Carbondale at the Electrical and Computer engineering department. I am working in the field of VLSI and Test Automation. Recently returned from a 9-month internship as analog circuit designer. Currently my research involves DFT algorithms and BIT circuits

11:00 am – 11:20 am Paper 2: "Calculating Signal Controllability using Neural Networks: Improvements to Testability Analysis and Test Point Insertion" Joshua Immanuel and Spencer K. Millican

This paper presents an artificial neural network-based signal probability predictor for VLSI circuits which considers reconvergent fan-outs. This study shows training and using artificial neural networks to predict signal probabilities increases post-test point insertion fault coverage compared to using COP, especially in circuits with many reconvergent fan-outs.

Presenting Author: Spencer K. Millican Auburn University
Dr. Millican is presently an Assistant Professor at Auburn University in Auburn, AL. He previously worked as a DFT engineer at the IBM Rochester Facility in Rochester, MN. His research interests include applying machine learning to DFT challenges and LBIST, and is the co-author numerous publications.

Industry Contributions 15 minutes and 5 minutes Q&A

11:20 am – 11:40 am Paper 3: "Verification and Testing Considerations of an In-Memory AI Chip" Marcia Golmohamadi, Ryan Jurasek, Wolfgang Hokenmaier, Don Labrecque, Ruoyo Zhi, Bret Dale, Nibir Islam, Dave Kinney, Angela Johnson

We present the testing and validation considerations for a programmable artificial neural network (ANN) integrated within a phase change memory (PCM) chip, featuring a Nor-Flash compatible serial peripheral interface (SPI). We introduce our method for validating the circuit components specific to the ANN application.

Presenting Author: Marcia Golmohamadi, Green Mountain Semiconductor
After finishing PhD's degree in Electrical Engineering at the University of Vermont in 2019, Marcia joined Green Mountain Semiconductor Inc. as a Circuit Design Engineer. Since then, she has been conducting research on development of a digital neuromorphic architecture to implement a programmable artificial neural

network (ANN) inside a memory die. Author and/or Co-author of 13 papers and publications.

11:40 am – 12:00 am Paper 4: "AI Powered THz VLSI Testing Technology"
Naznin Akter, Mustafa Karabiyik, Michael Shur, John Suarez and Nezih Pala

We present a new terahertz testing technique for non-destructive identification of genuine integrated circuits, in package, in-situ and either with no or under bias, by measuring their response to scanning terahertz and sub-terahertz radiation at the circuit pins. By establishing and AI processing of the THz scanning signatures of reliable devices and circuits and comparing these signatures with devices under test using AI, this technology could be used for reliability and lifetime prediction

Presenting Author: Michael Shur, Electronics of the Future Patricia W. and C. Sheldon Roberts Professor at RPI and co-founder of Sensor Electronics Technology, Inc., and of Electronics of the Future, Inc. He is Fellow of IEEE, APS, ECS, OSA, and SPIE and Fellow of the National Academy of Inventors and of several other professional societies. He is an IEEE EDS Distinguished Lecturer and Foreign Member of the Lithuanian Academy of Sciences.

12:00 am – 12:20 pm Paper 5: "Passive Intermodulation (PIM) Test and Measurement"
Stephen Moss, Elanchezhian Veeramani and Joris Angelo Sundaram Jerome

PIM is a form of intermodulation distortion that occurs in passive components. It is an unwanted signal created by the mixing of two or more RF signals, caused by the nonlinearity of the passive components in the RF path. The paper describes the way PIM measurements are performed and highlights how Multiband PIM measurements are carried out in a very efficient way.

Presenting Author: Elanchezhian Veeramani, GlobalFoundries
Presently RF Characterization Engineer, GlobalFoundries, Essex Junction, Vermont. Previously with Exalt Wireless, Dallas, Texas. 6 years of experience in RF test methods, RF amplifiers and transceiver hardware debugging, calibrations, measurements with test equipment and technical analysis of point to point microwave radios used in backhaul networks.

12:20 pm – 12:40 pm Paper 6: "Characterization of Thermal Runaway in a Ge Photodiode for Si Photonics" Stewart Rauch, *IEEE Life Fellow*, Dongho Lee, Alexey Vert, and Roy Gupta

The power limits due to thermal runaway of a geranium PIN photo diode as the O-band (1300nm wavelength) photo detector component of a silicon photonics technology were characterized under elevated stress conditions. A simplified model is used to project to use condition.

Presenting Author: Stewart Rauch, GlobalFoundries
Principal Member of Technical Staff at GlobalFoundries, NY, working in the areas of reliability of Si photonics and RF CMOS. Formerly he was a faculty member at State University of New York, New Paltz and a Senior Technical Staff Member at IBM Semiconductor Research and Development Center (NY), specializing in hot carrier, bias temperature instability, and soft error reliability of state of the art CMOS technologies. He is a Life Fellow of IEEE

12:40 pm – 1:00 pm Paper 7 "Self-heating characterization and its applications in technology development" P. Paliwoda, M. Toledano-Luque, T. Nigam, F. Guarin, M. Nour, S. Cimino, L. Pantisano, A. Gupta, O. H. Gonzalez, M. Hauser, W. Liu, A. Vayshenker, D. Ioannou, D. Lee, L. Jiang, P. Yee, S. Rauch and B. Min

This work presents various device self-heating temperature sensing techniques and discusses their application in device reliability projection. Details of sensor design, technology choice, layout and ambient temperature impact on measurement results are discussed

Presenting Author: Peter Paliwoda, GlobalFoundries

Peter received the B.S. and M.S. degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2003 and 2005, respectively, and the Ph.D. degree in electrical and computer engineering from the New Jersey Institute of Technology in 2018. He is with GLOBALFOUNDRIES, Malta, NY, USA, researching front-end-of-line reliability with an emphasis on metal gate/high-k CMOS/RF technologies and thermal characterization/modeling

Wednesday, June 24

(Presentation minutes are tentative and will be finalized close to but before June 24.)

10:00 am – 10:05 Welcome Address: Eugene Atwood General Chair

10:05 am – 10:10 Tutorial Introduction:
Krishna Chakravadhanula, Tutorial Chair, Carl Wisnesky, Vice Tutorial Chair

10:10 am – 10:40 Reliability, Availability, and Serviceability (RAS) - William J. Clarke (IBM)

Speaker Biography: William J Clarke is a senior engineer on the IBM Z RAS team with responsibility for high-end processors availability and service. He previously worked in logic design, engineering systems test and product engineering. He has co-authored multiple articles on RAS design.

Abstract: The system design team is the consumer of reliable circuit designs. The presentation will discuss circuit reliability from a consumer's point of view. System requirements and some methods used to achieve these requirements will be presented.

10:40 am – 11:10 Electronic Package Stress Testing and Reliability– Jeffrey T. Coffin (IBM)

Speaker Biography: Jeffrey T. Coffin received the B.S. degree in metallurgy and material science from the Columbia School of Engineering and Applied Sciences in 1983 and the M. S. degree in metallurgical engineering from the Polytechnic Institute of New York in 1986.He is a senior engineer at IBM, who has worked in the packaging reliability field since he joined the corporation in 1983. He holds several patents and has authored several papers related to electronic packaging technologies.

Abstract: It has been widely recognized that Moore's Law has reached its limit based solely on device scaling. Additionally, each node drives higher and higher fabrication costs with diminishing performance returns, so technologists are turning to other means to maintain continual improvements. Advanced packaging technologies are one of the approaches being effectively utilized. While the reliability of the package and interconnections has always been an industry focus, continued vigilance is required as smaller package feature scaling increases risk, functional integration of the package increases, and new package technologies are developed and introduced to volume production. A wide variety of packaging options are becoming commercially available to improve system performance. This presentation describes the design for reliability considerations for the package, and testing methodology to demonstrate and assure packaging reliability.

11:10 am – 11:40 Better Accelerated Testing – Dr. Wayne Nelson (Private Consultant)

Speaker Biography: Dr. Nelson is a leading expert on reliability data analysis, recurrent-events data analysis, and statistical methods for accelerated testing. Before becoming a private consultant in 1989, he was an employee of General Electric Corp. Research & Development for 24 years and consulted across the company. Dr Nelson also provides expertise as an expert witness.

Abstract: This talk describes recent advances in statistical models and data analyses and plots for accelerated tests. Using these advances, scientists and engineers can run better tests that are faster and more efficient, informative, and accurate. Better tests are illustrated with a variety of applications including microprocessors, solid state devices, electrical insulation, metal fatigue, lubricating oil, electromigration failure of microcircuit conductors, and more.

11:40 am – 12:10 Physics of Failure and the Dangers of Overstressing
- Dr. James R. Lloyd (SUNY Polytechnic Institute)

Speaker Biography: Presently Lecturer and Adjunct Professor SUNY Polytechnic Institute, Albany NY. Previously with IBM T.J. Watson Research Laboratory, Yorktown Heights NY, Jet Propulsion Laboratory,

Pasadena CA, Digital Equipment Corporation Hudson MA, Max Planck Institut fuer Metallforschung, Stuttgart, Germany and IBM East Fishkill Facility. More than 40 years of experience in Semiconductor Reliability physics. Author and/or Co-author of approximately 100 papers and publications.

Abstract: To determine the anticipated reliability of a semiconductor, accelerated testing is necessarily used. Devices are exposed to conditions more severe than the operational use conditions in order to excite failure mechanisms in practical time frames for the engineer.

This tutorial will review the physical limitations for accelerated reliability testing to avoid overstressing for the major semiconductor failure modes and mechanisms. Electromigration, TDDB (Time Dependent Dielectric Breakdown) Stress voiding will be concentrated on followed by discussions about the other failure mechanisms semiconductor devices are prey to.

12:10 pm – 12:40 Panel *"Achieving Semiconductor Reliability: Without Burn-In."*

Malinky Ghosh (IBM) Panel Chair, Jim Lloyd (SUNYPOLY) Moderator,
Panelists: William J. Clarke, Jeffrey T. Coffin, Dr. Wayne Nelson, Dr. James R. Lloyd

Abstract: The practice of burning in semiconductor devices, in particular, assemblies of devices known as Systems On a Chip (SOC), is becoming increasingly difficult. Managing the amount of power dissipated by the SOC at elevated voltage and temperature is very challenging. Maintaining uniform temperature across the chip and ensuring that all logic participates in so called 'toggle coverage' to prevent over aging of chip regions or devices is difficult. EDA tools do not support toggle coverage evaluation or management of many different IP domains over the burn-in duration. Sending SOC material into burn-in, some of which subsequently fails, forces incoming test and post burn-in test to be high quality.
Given that reliability statistics encompass the population of material, a method which eliminates or minimizes burn-in effort and improves the reliability statistics of the population is valuable, provided the method costs less than the cost of burn-in plus burn-in scrap. Several methods have been published {1-6] which address methods to minimize semiconductor dependence on burn-in. In addition to predictive methods, system designs are including real-time monitoring methods to identify failing memory or logic elements where the system responds by applying redundancy or partitioning the failing logic outside of the functional operating space of the system. Redundancy and isolation have a cost in terms of requiring additional silicon or reduced performance, respectively.

The circumstances suggest that a best solution would be using in-line silicon with unique easy to test structures which predict the reliability of nearby material. Enhanced predictive methods which combine in-line based predictions with SOC test results and system redundancy suggest a robust cost effective path forward to reduce or eliminate traditional burn-in.

Panel Format: The panelists will be asked to respond to a series of questions. Audience members may ask questions using the 'chat' feature of Zoom or ahead of time by communicating with the NATW panel chair, Malinky Ghosh. This section of the agenda is expected and encouraged to run overtime.