CHALLENGES AND OPPORTUNITIES FOR SUB-5NM MACHINE LEARNING ACCELERATORS AND HARDWARE SECURITY TECHNOLOGIES

Dr. Ram K. Krishnamurthy, Senior Research Director and Senior Principal Engineer
Intel Labs, Intel Corporation, Hillsboro, OR, USA

Abstract: This presentation will highlight some of the emerging challenges and opportunities for sub-5nm in-memory/near-memory AI computing, machine learning accelerators, and hardware security technologies in the rapidly evolving AI and IoT industries. With Moore's law process technology scaling well into the nano-scale regime, future SoC platforms ranging from high performance cloud servers to ultra-low-power edge devices will demand advanced AI capabilities and stronger security features. New and emerging IoT markets for autonomous vehicles, drones, and wearables require even higher performance and security at much lower cost while reducing energy consumption. Some of the prominent barriers to designing high performance and energy-efficient AI and security engines in multi-core microprocessors and SoCs will be outlined. New paradigm shifts necessary for implementing in-memory and near-memory compute functions and integrating special-purpose machine learning accelerators and hardware security processors into next-generation SoCs will be presented. Specific chip design examples and case studies supported by silicon measurements and trade-offs will be discussed.

Biography: Ram K. Krishnamurthy received the B.E. degree in electrical engineering from the National Institute of Technology, Trichy, India, in 1993, the M.S. degree in electrical and computer engineering from the State University of New York, Buffalo, NY, USA, in 1994, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1997. He has been at Intel Corporation since 1997. He is currently a Senior Research Director and Senior Principal Engineer at Intel Labs, Hillsboro, OR, USA, where he heads the High Performance and Low Voltage Circuits Research Group. In this role, he leads research in high performance, energy-efficient, and low-voltage circuits for next generation microprocessors, accelerators, and Systems-On-Chip (SoCs). He has led circuit technology research directions in high speed arithmetic units, on-chip interconnects, reconfigurable computing, energy efficient clocking, ultra low voltage design, hardware security, compute-in-memory, neuromorphic computing, and machine learning accelerators. He has made circuit technology contributions to multiple generations of Intel's data center, client, FPGA, IoT, and AI products spanning across 180nm to 7nm process technology nodes. Krishnamurthy has filed 320 patents and holds 180 issued patents. He has published 200 papers and four book chapters on high-performance and energy-efficient circuits. He serves as the Chair of the Semiconductor Research Corporation (SRC) Technical Advisory Board for the circuit design thrust. He served as the Technical Program Chair and the General Chair of the IEEE International Systems-on-Chip Conference and presently serves on the Conference's Steering Committee. He is an Adjunct Faculty with the Electrical

and Computer Engineering Department, Oregon State University, Corvallis, OR, USA, where he taught advanced VLSI design. Krishnamurthy has received two Intel Achievement Awards for pioneering the first 64-bit Sparse-Tree ALU Technology and the first Advanced Encryption Standard hardware security accelerator on Intel products. He has received the IEEE International Solid State Circuits Conference Distinguished Technical Paper Award, IEEE European Solid State Circuits Conference Best Paper Award, Outstanding Industry Mentor Award from SRC, Intel awards for most patents filed and most patents issued, Intel Labs Gordon Moore Award, Alumni Recognition Award from Carnegie Mellon University, Distinguished Alumni Award from the State University of New York, MIT Technology Review's TR35 Innovator Award, and was recognized as a top ISSCC paper contributor. He has served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society, a Guest Editor of the IEEE Journal of Solid State Circuits, an Associate Editor of the IEEE Transactions on VLSI Systems, and on the Technical Program Committees of ISSCC, CICC, and SOCC conferences. He is a Fellow of the IEEE and a Board Member of the Industry Advisory Board for the State University of New York.