2021 IEEE Microelectronic Design and Test Symposium

Virtual, by Zoom, Agenda

The 30th IEEE Microelectronics Design & Test Symposium (MDTS, formerly known as NATW) provides an annual world forum for academy and industry researchers and engineers to discuss latest advances in microelectronics, share their visions in modern microelectronic technologies and foster academy-industry collaboration. The four-day symposium will feature keynote and plenary talks, special sessions, tutorials. The MDTS'2021 will be a full virtual event holding sessions from 10AM to Noon, Networking ZOOM lunch 12:10PM to 12:50PM, 1PM to 3PM on May 18 through May 21.

MDTS-2021 is sponsored by IEEE Schenectady Section and IEEE Region 1, and is supported by IBM Corp., Advantest America, AdamsIP, Mentor (A Siemens Business), Cadence Design Systems, Green Mountain Semiconductor and OnSemiconductor.

Tuesday, May 18

Session 1 : Tutorial

10:00 am – 10:10am Welcome Address: Eugene Atwood General Chair

10:10 am – 10:15 am Tutorial Introduction:
Krishna Chakravadhanula, Tutorial Co-Chair, Carl Wisnesky, Tutorial Co-Chair

10:15 am – 10:55 am - "Security – From Simple Encryption to Secure System with Root of Trust and Anti Tamper Technology"

Speaker: Tomas Eckenrode - Alion Science & Technology
Thomas Eckenrode is currently at Alion Science & Technology and just completed a NoC design for signal processing application. He is currently developing techniques for secure radar pulse word descriptor tracking and researching various physically unclonable function (PUF) technology for key generation and other functions. Tom has over 20 years experience in designing, architecting, and managing complex micro-processor and secure processor system designs. He has implemented secure anti-tamper solutions on several systems and developed data at rest and in-flight encryption architectures for Flash based array servers.

Abstract: What is Cyber security, how do you decide what to secure, how much do you invest in security, what system performance loss is acceptable to make a system secure, when do I start thinking about security, Is it a winnable game. These are some of the many questions asked when incorporating security into a system. Security can be as simple as encrypting a file or as complex from bootup to secure processing using the latest Anti-Tamper, Monitoring, Obfuscation, counterfeit checking, and Forensic concepts when operating in a Root of Trust (RoT) environment. This presentation is intended to give a summary of the many elements that are incorporated into a secure system and the thought process of designing a secure system. The talk briefly covers Extension of Security (EoS), Root of Security (RoS), Root of Processing (RoP) and the NIST Cybersecurity Framework. Along with an example of what should be considered when designing security into a product. The discussion is intended as a high-level overview of security and the many aspects of it and not a math intensive deep dive into the cryptographic and hashing algorithms.

10:55 am – 11:35 am - "Physical Assurance and Inspection on Electronics"

Speaker: Dr. Navid Asadi - Florida Institute for Cybersecurity (FICS) Research
Dr. Navid Asadi is an assistant professor in the Department of Electrical and Computer Engineering at the University of Florida. His research is mainly focused on physical inspection of electronics from device to system level. He investigates novel techniques for electronics counterfeit detection/prevention, system and chip-level reverse engineering, anti-reverse engineering, invasive and semi-invasive physical attacks, integrity analysis, etc. He has received several best paper awards and is the co-founder of the IEEE-PAINE Conference.

Abstract: Globalization has made the semiconductor industry more susceptible to trust and security issues. Hardware Trojans, i.e., malicious modification to electronic systems, can violate the root of trust when the device or systems are fabricated/assembled in untrusted facilities. As the imaging and failure analysis tools excel in the resolution and capability, physical inspection-based methods become more attractive in verifying such trust issues. On the contrary, such physical inspection methods are opening new capabilities for an adversary to extract sensitive information like secret keys, memory content or intellectual property (IP) compromising confidentiality and integrity. Different countermeasures have been proposed, however, there are still many unanswered questions. This talk will focus on the state-of-the-art physical inspection/assurance methods, the existing countermeasures, related challenges to develop new countermeasures and a research roadmap for this emerging field.

11:35 am – 12:15 pm - "On-Demand Key Generation to Secure Blockchains with Tamper Resistant ReRAMs"

Speakers: Dr. Bertrand Cambou and Dr. Fatemeh Afghah - Northern Arizona University
Dr. Bertrand Cambou is a Professor at Northern Arizona University (NAU) in nanoelectronics and cybersecurity. He is the Principal Investigator (PI) of a $6,000,000 program funded by the Air Force Research Laboratory (AFRL) to use nanotechnologies for cybersecurity, and quantum cryptography. With 100 granted and pending patents, he is an Invention Ambassador of the American Association for the Advancement of Science (AAAS), and a senior member of the National Academy of Inventors (NAI). He worked as a senior executive and a technologist in the cybersecurity industry at Gemplus and Ingenico, and in microelectronics at Advanced Micro Devices (AMD), Motorola, Silicon Storage Technology (SST), and Crocus Technology. At Motorola he was a distinguished innovator, and a scientific advisor of the corporation's Board of Directors. He was nominated by IBM and Motorola as the Director of the Somerset Power PC microprocessor design center, in support of Apple Computer. He holds a Doctorate degree in Electronics and Material Science from Paris-Saclay University, an Electrical Engineering degree from Supelec-Paris, and a Master degree in Physics from Toulouse-III University.

Abstract: Protocols based on the generation of new public-private key pairs to digitally sign each blockchains has been demonstrated with physical unclonable functions (PUFs) [1]. The loss of the keys is not anymore important as they are only used once. However the security of such protocols can be compromised when the opponent gets physical access of the PUFs and is able to read the content of the devices. We will present the development of a solution generating key pairs on demand from Resistive Random Access Memories (ReRAM) operating in the nA range, well below the formation of the conductive filaments needed to enable the usual programing-read-erase cycles. The key pairs are generated in a few milliseconds. These devices operate below noise level, thereby mitigating side channel analysis. We will also discuss how attempts by third parties to directly read the devices are likely to damage the PUFs and leave non-erasable traces. In case of the detection of an attack, the ReRAM PUFs can be permanently destroyed with nano joules of power in milliseconds.

12:15 pm - 1:15 pm Lunch

Session 2 : Tutorial Continued

1:15 pm – 1:55 pm - "New Frontiers of Hardware Security in the IoT Regime"
Speaker: Dr. Swarup Bhunia - Semmoto Endowed Professor of IoT, Electrical and Computer Eng., University of Florida, Gainesville, Florida

Dr. Swarup Bhunia is currently a preeminence professor of cybersecurity and Semmoto Endowed Professor of IoT at University of Florida. He serves as the Director of the Warren B. Nelms Institute for the Connected World. Earlier, he was appointed as the T. and A. Schroeder associate professor of Electrical Engineering and Computer Science at Case Western Reserve University. He has over twenty years of research and development experience with 300+ publications in peer-reviewed journals and premier conferences and ten authored/edited books. His research interests include hardware security and trust, adaptive nanocomputing and novel test methodologies. Dr. Bhunia received IBM Faculty Award (2013), National Science Foundation career development award (2011), Semiconductor Research Corporation Inventor Recognition Award (2009), and SRC technical excellence award (2005) as a team member, and several best paper awards/nominations. He is co-founding editor-in-chief of a Springer journal on hardware and systems security. Dr. Bhunia received his PhD from Purdue University on energy-efficient and robust electronics.

Abstract: With the emergence of the Internet of Things (IoT) regime that promises exciting new applications from smart cities to connected autonomous vehicles, security has come to the forefront of the system design process. Recent discoveries and reports on numerous security attacks on microchips and circuits violate the well-regarded concept of hardware trust anchors. It has prompted system designers to develop design-for-security and test/validation solutions to achieve secure electronic hardware. Emerging security issues and countermeasures have also led to interesting interplay between security, verification, and interoperability. Verification of hardware for security and trust has become an integral part of the system design flow. The talk will cover the spectrum of challenges associated with IoT security and describe emerging solutions in creating secure trustworthy hardware that can enable IoT security for the mass. It will outline the need and challenges for verification of electronic designs for security properties and the motivation for learning-guided security design and verification.

1:55 pm - 2:00 pm Break

2:00 pm - 2:05 pm Keynote Introduction: Danella Zhao

2:05 pm - 3:05 pm Keynote: Challenges and opportunities for sub-5nm machine learning accelerators and hardware security technologies

Speaker: Dr. Ram Kumar Krishnamurthy, Senior Research Director and Senior Principal Engineer, Intel Labs, Intel Corporation, Hillsboro, OR, USA

Abstract: This presentation will highlight some of the emerging challenges and opportunities for sub-5nm in-memory/near-memory AI computing, machine learning accelerators, and hardware security technologies in the rapidly evolving AI and IoT industries. With Moore's law process technology scaling well into the nano-scale regime, future SoC platforms ranging from high performance cloud servers to ultra-low-power edge devices will demand advanced AI capabilities and stronger security features. New and emerging IoT markets for autonomous vehicles, drones, and wearables require even higher performance and security at much lower cost while reducing energy consumption. Some of the prominent barriers to designing high performance and energy-efficient AI and security engines in multi-core microprocessors and SoCs will be outlined. New paradigm shifts necessary for implementing in-memory and near-memory compute functions and integrating special-purpose machine learning accelerators and hardware security processors into next-generation SoCs will be presented. Specific chip design examples and case studies supported by silicon measurements and trade-offs will be discussed.

Biography: Ram K. Krishnamurthy received the B.E. degree in electrical engineering from the National Institute of Technology, Trichy, India, in 1993, the M.S. degree in electrical and computer engineering from the State University of New York, Buffalo, NY, USA, in 1994, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1997. He has been at Intel Corporation since 1997. He is currently a Senior Research Director and Senior Principal Engineer at Intel Labs, Hillsboro, OR, USA, where he heads the High Performance and Low Voltage Circuits Research Group. In this role, he leads research in high performance, energy-efficient, and low-voltage circuits for next generation microprocessors, accelerators, and Systems-On-Chip (SoCs). He has led circuit technology research directions in high speed arithmetic units, on-chip interconnects, reconfigurable computing, energy efficient clocking, ultra low voltage design, hardware security, compute-in-memory, neuromorphic computing, and machine learning accelerators. He has made circuit technology contributions to multiple generations of Intel's data center, client, FPGA, IoT, and AI products spanning across 180nm to 7nm process technology nodes. Krishnamurthy has filed 320 patents and holds 180 issued patents. He has published 200 papers and four book chapters on high-performance and energy-efficient circuits. He serves as the Chair of the Semiconductor Research Corporation (SRC) Technical Advisory Board for the circuit design thrust. He served as the Technical Program Chair and the General Chair of the IEEE International Systems-on-Chip Conference and presently serves on the Conference's Steering Committee. He is an Adjunct Faculty with the Electrical and Computer Engineering Department, Oregon State University, Corvallis, OR, USA, where he taught advanced VLSI design. Krishnamurthy has received two Intel Achievement Awards for pioneering the first 64-bit Sparse-Tree ALU Technology and the first Advanced Encryption Standard hardware security accelerator on Intel products. He has received the IEEE International Solid State Circuits Conference Distinguished Technical Paper Award, IEEE European Solid State Circuits Conference Best Paper Award, Outstanding Industry Mentor Award from SRC, Intel awards for most patents filed and most patents issued, Intel Labs Gordon Moore Award, Alumni Recognition Award from Carnegie Mellon University, Distinguished Alumni Award from the State University of New York, MIT Technology Review's TR35 Innovator Award, and was recognized as a top ISSCC paper contributor. He has served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society, a Guest Editor of the IEEE Journal of Solid State Circuits, an Associate Editor of the IEEE Transactions on VLSI Systems, and on

the Technical Program Committees of ISSCC, CICC, and SOCC conferences. He is a Fellow of the IEEE and a Board Member of the Industry Advisory Board for the State University of New York.

Wednesday, May 19

Session 3

10:00 am – 10:05 am Welcome: Eugene Atwood General Chair

10:05 am – 10:10 am Keynote Introduction: Brion Keller

10:10 am – 11:10 am Keynote: CAD for (SoC) Security: Pre-silicon Security Sign-off from C to GDSII
Speaker: Mark Tehranipoor, University of Florida

Abstract: SoC security has received significant attention over the past few years. Automation, metrics, standards, and development of computer-aided design (CAD) solutions to provide pre-silicon security vulnerability extraction and countermeasure is still a work in progress. There are numerous security vulnerabilities that must be identified through the course of the design process and addressed before the design is sent for fabrication. Examples include power and EM side channels, fault injection, information leakage, access control, and more. This talk discusses the challenges in developing CAD for SoC security, and presents sample solutions to provide countermeasure at various stages of the design process.

Biography: Mark Tehranipoor is currently the Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity at the ECE Department, University of Florida. He is also currently serving as Director for Florida Institute for Cybersecurity Research (FICS), National Microelectronics Security Training Center (MEST), CYAN Center of Excellence, and ECI Transition Center. His current research interests include: IoT security, hardware security and trust, supply chain risk management and security, counterfeit electronics detection and prevention and reliable circuit design. Dr. Tehranipoor has published extensively in the field of hardware security and has delivered more than 200 invited talks and keynote addresses. He has 8 patents, and has published 13 books and 22 book chapters. He is a recipient of 13 best paper awards and nominations, as well as the 2008 IEEE Computer Society (CS) Meritorious Service Award, the 2012 IEEE CS Outstanding Contribution, the 2009 NSF CAREER Award, and the 2014 MURI award. His projects are sponsored by both the industry and Government.
He serves on the program committee of more than a dozen leading conferences and workshops. He served as Program and General Chairs of several leading conferences and workshops. He co-founded a new symposium called IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) and served as HOST-2008 and HOST-2009 General Chair (http://www.hostsymposium.org/). He is currently serving as HOST's Chair of Steering Committee. He is also the co-founder of Trust-Hub (www.trust-hub.org) and Asian HOST (http://asianhost.org/2017/). He serves as co-EIC for newly established Journal on Hardware and Systems Security (HaSS). He also served as an Associate EIC for IEEE Design & Test, an IEEE Distinguished Speaker, and an ACM Distinguished Speaker from 2010 to 2014. He is currently serving as an Associate Editor for JETTA, JOLPE, Transactions on VLSI (TVLSI), and Transactions on Design Automation for Electronic Systems (TODAES). Prior to joining University of Florida, Dr. Tehranipoor served as the founding director of the Center for Hardware Assurance, Security, and Engineering (CHASE) and the Comcast Center of Excellence in Security Innovation (CSI) at the University of Connecticut. Dr. Tehranipoor is a Fellow of IEEE, a Golden Core Member of the IEEE, and Member of ACM and ACM SIGDA. He is currently serving as IEEE Ambassador on Cybersecurity

Break 11:10 am- 11:15 am

11:15 am – Noon Invited: Structural test challenges in achieving cost-effective automotive quality
Speaker: Devanathan Varadarajan, Senior Member Technical Staff / Design Manager, Texas Instruments Inc., USA

Abstract: Automotive applications pose stringent constraints on SoCs to support very low failure/FIT rates, very high quality of near-0 DPPM (defective parts per million), and long operational lifetimes withstanding a wide range of temperatures (-40C to 125C/150C). With automotive markets mandating in-field tests, ATE manufacturing tests and in-field system test have different objectives with respect to addressing DPPM and FIT targets, respectively. Further, with increasing use of diverse high-performance IP cores in automotive SOCs, power-performance-area

overhead with test logic is becoming prominent impacting the overall cost of the device. In this talk, case-studies are presented to address the above challenges to ensure cost-effective automotive quality.

Biography: Devanathan Varadarajan is a Senior Member Technical Staff and Design Manager at Texas Instruments with expertise in the areas of test quality and test cost optimizations across digital logic, embedded memory and analog components. He has been with TI since 2003 and has a PhD from Indian Institute of Technology, Madras.

Noon – 1:00 pm Lunch

Session 4

Special Session: Innovations In Optical Computing Organizer: Eugene Atwood

1:00 pm – 1:40 Session 4.1: Photonic Computing for Transformative AI, Igor Carron, Lighton

Abstract: The emergence of Large Language Models that require no fine-tuning and only a few demonstrations to understand tasks and perform them, has recently taken the world of Artificial Intelligence by surprise. This transformative AI has also fueled a quest for larger such models that may include multimodalities (images, videos). The downside of these models resides in the vast amount of computations required to train them and to make inferences with them. For instance, with 175 billion parameters, training OpenAI GPT-3 is thought to have required the equivalent of a month of continuous computing time of several thousand high-end GPUs. In this talk, we will show how, at LightOn, we are devising a photonic computing hardware technology in tandem with new algorithms to train present and future Large Scale AI Models.

Speaker Biography: Igor Carron is the CEO and co-founder of LightOn a start-up company based in Paris, France. Over the years, Igor has developed expertise in leading engineering groups in complex engineering projects (Nuclear and Aerospace). He is the writer of a blog on Compressive Sensing and Machine Learning that garnered more than 8 million views. Since 2013, he has organized the Paris Machine Learning meetup with over 100+ meetups, 300+ speakers, and 8000 members. Igor has a diplôme d'ingénieur from INPG, Grenoble, France, and a Ph.D. from Texas A&M University.

1:40 pm – 2:20 pm Session 4.2: Photonic convolutional processors and optical crossbars for neural network training, Bert Offrein, IBM Research

Abstract: With the proliferation of ultrahigh-speed mobile networks and internet-connected devices, along with the rise of artificial intelligence (AI)1, the world is generating exponentially increasing amounts of data that need to be processed in a fast and efficient way. Highly parallelized, fast and scalable hardware is therefore becoming progressively more important. Here we demonstrate a computationally specific integrated photonic hardware accelerator (tensor core) that is capable of operating at speeds of trillions of multiply-accumulate operations per second 10^12 MAC operations per second or tera-MACs per second. The tensor core can be considered as the optical analogue of an application-specific integrated circuit (ASIC). It achieves parallelized photonic in-memory computing using phase-change-material memory arrays and photonic chip-based optical frequency combs (soliton microcombs). The computation is reduced to measuring the optical transmission of reconfigurable and non-resonant passive components and can operate at a bandwidth exceeding 14 gigahertz, limited only by the speed of the modulators and photodetectors. Given recent advances in hybrid integration of soliton microcombs at microwave line rates, ultralow-loss silicon nitride waveguides, and high-speed on-chip detectors and modulators, our approach provides a path towards full complementary metal–oxide–semiconductor (CMOS) wafer-scale integration of the photonic tensor core. Although we focus on convolutional processing, more generally our results indicate the potential of integrated photonics for parallel, fast, and efficient computational hardware in data-heavy AI applications such as autonomous driving, live video processing, and next-generation cloud computing services**.**

Speaker Biography: Bert Offrein received his Ph.D. degree in nonlinear integrated optics from the University of Twente (NL) in 1994. He then joined IBM Research - Zurich and contributed to establishing and commercializing adaptive integrated optical technology for DWDM networks. From 2004 to 2016, Bert Offrein was managing the photonics group, addressing optical interconnects for computing systems. Since 2016, he is leading the neuromorphic devices and systems group, focusing on novel hardware for neural networks. Bert Offrein is a principal research staff member at IBM Research and the co-author of over 150 publications and the co-inventor of more than 35 patents.

2:20 pm - 2:25 pm Break

2:25 pm – 3:05 pm Session 4.3: Processing Acceleration using Optical Fourier Transform, Iman Kundu, Optalysys Ltd

Abstract: We present a novel approach in optical processing by accelerating Fourier transform through integration of silicon photonics and free-space optics. We introduce Fourier transform based multiply and accumulate operations, that require less number of operations compared to the traditional multiply and accumulate operations used in computer architecture. The significant reduction in the number of operations, predicts the ETile to be a universal accelerator for any AI/big data hardware.

Speaker Biography: Iman Kundu received the B.Tech degree in electronics and communication engineering from the West Bengal University of Technology, Kolkata, India, in 2007, and the M.Sc (ENG.) degree in nanotechnology and advanced electronic devices and the Ph.D. degree in electronic and electrical engineering from the University of Leeds, Leeds, U.K., in 2010 and 2014, respectively. From 2008-2009, he was an assistant systems engineer with the Tata Consultancy Services, India, working on software development. From 2014-2019, he has been a Post-Doctoral Research Fellow with the University of Leeds, UK. Since 2019, he is the Photonics Scientist at Optalysys Ltd. His research interest includes the development of photonic integrated circuits for different wavelengths from far-infrared to near-infrared, ultrafast laser dynamics, laser feedback interferometry, fabrication of micro- and nano-structures on far-infrared laser waveguides, Fourier optics, and development of optical accelerators for AI.

Thursday, May 20

Session 5

10:00 am – 10:05 am Welcome: Eugene Atwood General Chair : Introduction of David Yeh

10:05 am – 10:50 am Invited: Decadal Plan for Semiconductors - the New Roadmap
Speaker: David Yeh, Senior Director, and John Oakly, Science Director, Semiconductor Research Corporation

Abstract: For over the past year, semiconductor industry and government agency thought leaders in electronics have met to discuss the need for research in the coming decade. The result is the SRC Decadal Plan for Semiconductors and they describe five seismic shifts that will influence electronics over the coming decade. Significant research is needed to address the challenges of the shifts and industrial companies who successfully navigate the coming changes will be positioned to dominate the marketplace. Governments also have a stake in this effort – national competitiveness issues abound, as well as individual security and privacy concerns. The presentation will discuss some of the ramifications of the document and how it might impact research funding around the world.

Biography: Dr. Yeh is currently a Texas Instruments assignee at the Semiconductor Research Corporation, where he is senior director and manages four research programs: i) Analog/Mixed-Signal Circuits, Systems, and Devices, ii) Artificial Intelligence Hardware; iii) Computer-aided Design and Test; iv) and the India Research Program. In his position he funds and supports university research projects addressing high-speed, low-power, robustness, and manufacturability issues in the integrated circuit design space for digital, analog, mixed-signal, and RF products. He also funds and supports university research to enable neuro-inspired, cognitive and learning abilities which address the vast range of future data types and workloads as intelligence is enabled from edge devices to the cloud. He also funds and supports university research addressing computer-aided design algorithms and testability issues used in the design and manufacturing of integrated circuits. Finally, he funds and supports university research projects in India, on behalf of the members who have a presence in that country. Dr. Yeh joined Texas Instruments in 1990 and has been elected as a Senior Member Technical Staff. He has held positions in the Semiconductor Process and Device Center, Design Automation Division, High Performance Analog, and Analog Technology Development groups. He is a Senior Member of IEEE, and is a graduate of the University of Illinois at Urbana-Champaign (BS, MS, Ph.D).

Biography: John Oakley, a Science Director at SRC, is focused on leading Hardware Security (HWS), Packaging (PKG), Automotive Electronics (Auto), and Intelligent Cognitive Assistant (ICA) research. John works closely with government, industry, and university partners to advance these research topics. John was formerly a RF Control Architect at Intel Corporation, has over 20 years of successful digital design experience at Motorola, Freescale, Fujitsu, and Intel. His willingness to help and mentor, in addition to his deep technical expertise, make him a key member of Intel's technical team. John has 14 issued patents and has developed more than 55 successful integrated devices, several of which have shipped in high volumes. He has worked in numerous digital system spaces, and is presently in the transceiver and modem fields focusing on the control planes of cellular platforms. An expert in 3GPP standards and their application to real world devices, John was Vice Chairman of the MIPI Working Group RFFE and a member of the MIPI Working groups RIO and TSG. Beyond the work environment, John is a Ruby Life Master at Bridge and is an avid player of strategy and role playing games.

Break 10:50 am - 11:00 am

11:00 am -11:05 am **Program Introduction**
Danella Zhao, Old Dominion University

Papers Session A: Machine Learning for Testing & Reliability

Session Chair: Tian Xia **Session Co-chair: Paul Reuter**

11:05 am – 11:25 am Paper Session A.1: Sanmitra Banerjee, Duke Univ
Title: Towards Functionally Robust AI Accelerators
Abstract: Recent advances in deep learning can be attributed to the continued performance improvement of hardware processors and artificial intelligence (AI) accelerators. In addition to conventional CMOS accelerators based on Von Neumann architecture, emerging technologies such as silicon photonics, memristors, and monolithic 3D (M3D) integration are being explored as post-Moore's law alternatives. However, the energy efficiency and performance of emerging AI accelerators can be catastrophically impacted by faults due to fabrication-process

variations, thermal crosstalk, and aging. In this paper, we analyze the performance of several emerging AI accelerators in the presence of different uncertainties, and present low-cost methods to assess the significance of faults and mitigate their effects. We show that across all technologies, the impact of uncertainties on the performance can vary significantly based on the fault type and the parameters of the affected component. Therefore, the fault criticality-assessment techniques presented in this paper are necessary for yield improvement.

11:25 am – 11:45 am Paper Session A.2: Soham Roy, Auburn Univ.
Title: Principal Component Analysis in Machine Intelligence-Based Test Generation
Abstract: In a machine intelligence (MI)-based automatic test pattern generator (ATPG), an artificial neural network (ANN) may guide decisions that would otherwise rely on some heuristic. Heuristics use circuit-specific data such as gate types, logic depth, fan-out data, or various testability measures. Treating these data collectively as a multivariate statistic of circuit topology, this study extracts principal components (PCs) and a subset of PCs is then used to train an ANN and facilitates algorithmic decisions in the ATPG. This reduces the ANN complexity and enhances ATPG efficiency. Results on benchmark circuits show benefits to reduced CPU time.

11:45 am – 12:05 pm Paper Session A.3: Xiang Chen, Huawei Tech, China
Title: A Machine Learning-based Approach for Failure Prediction at Cell Level based on Wafer Acceptance Test Parameters
Abstract: Wafer Acceptance Test (WAT) or commonly known as Process Control Monitoring (PCM) includes numerous testing items that have many important applications, such as yield improvement and production cost control. The prediction of wafer yield based on WAT parameters has been successfully employed to reduce production costs spent on the circuit probing process. However, the relationship between WAT and subsequent diagnostic reports has not been sufficiently explored yet. This paper proposes a learning-based framework for failure prediction at cell level from WAT data, including various techniques for feature selection and handling imbalanced classes. Based on the selected parameters, machine learning models are employed to predict the failure of a given cell. The potential of the proposed methodology is evaluated over a set of industrial data. Experimental results demonstrate that our methodology can provide accurate test predictions (0.95+ accuracy, F1-score, and Area Under the Receiver Operating Characteristic curve (AUC-ROC)).

12:05pm – 1:00 pm Lunch

Papers Session A: Machine Learning for Testing & Reliability

1:00 pm – 1:20 pm Paper Session A.4: Minsoo Kim, Sungkyunkwan Univ, South Korean
Title: Detection of Field Failure Chips by Ensemble Learned from Different Chip Areas
Abstract: Defect detection using machine learning techniques in semiconductor manufacturing has been known to be a very difficult problem owing to two issues: a very smaller number of defectives compared to the number of well-functioning chips and an invisible feature difference between fail and pass chips. The former corresponds to the class imbalance problem and the latter implies the class overlap in the context of classification. This research attempts to overcome these difficulties by proposing a new ensemble learned from different chip areas. Considering that physically close chips each other have similar characteristics, we split a wafer into radial and pie-shaped areas and construct an ensemble of classifiers, where each of those is learned from only one area data. The intuition behind this idea is that the fail and the pass classes can be separable in a specific area, which would be beneficial to successful failure detection. The numerical experiments based on three real world datasets from a semiconductor manufacturer verified the effectiveness of the proposed method.

Paper Session B: Electronics Test Methodologies & EDA Tools

Session Chair: Andrew Laidler Session Co-chair: Uma Srinivasan

1:20 pm – 1:40 pm Paper Session B.1: Mohammad Reza Naeemi Khaledi, Univ, Iran
Title: Compensating Detection Latency of FPGA Scrubbers with a Collaborative Functional Hardware Duplication
Abstract: Scrubbing is an effective FPGA error detection and correction method for configuration memory's faults. Scrubbing, however, is a serial procedure with several milliseconds latency. This latency may allow some errors to affect the system functionality. To prevent this effect, we have devised our duplication method of reliability operating in parallel and hand-in-hand with scrubbing to recover from errors. Our experiments results demonstrate that mean time to failure (MTTF) is improved by 966% and 150% over the pure scrubbing and triple modular redundancy (TMR), respectively. Additionally, our method enters the safe fail procedure in the remaining cases.

1:40 pm – 2:00 pm Paper Session B.2: Nicholai R L'Esperance, IBM, Cadence
Title: High Throughput Multiple Device Chain Diagnosis Methodology for Clock and Control Line Defects
Abstract:Accuracy and throughput are the most important considerations for any scan-based diagnosis methods. When chain tests fails on an Integrated Circuit (IC), massive failures must be logged to perform software-based chain diagnosis. Moreover, failing chain tests indicate the presence of defects not just on the scan path, but also on global signals such as clocks and control signals. For a successful volume diagnosis of chain failures, a methodology that can work with minimal failure logging and yet accurately identify the defect locations with high throughput is desirable. In this paper, we propose a production proven scan chain diagnosis methodology based on multiple device diagnosis (MDD) that makes use of a Design for Diagnosis (DFD) technique and accurately identifies clock and control signal defects in addition to defects on scan-path. Accuracy results of the proposed methodology is proven through Physical Failure Analysis (PFA) on silicon, and the run time of the proposed algorithm achieved up to 19X speed-up over the incumbent approach.

2:00 pm - 2:05 pm Break

2:05 pm – 2:25 pm Paper Session B.3: John G Massey, IBM
Title: Large-Scale Thermal TCAD Simulations of 7nm Circuits
Abstract: Many IC thermal simulations use only a small volume due to machine/EDA tool constraints. This work presents a thermal TCAD simulation methodology on a large-scale 7nm circuit using available thermal TCAD tools. The circuit model is based on a 3 x 3 array of inverter circuits and incorporates 18 metal levels in the back-end. A constant power is applied to each channel of the devices in the inverters as the heat source. The steady-state temperature is calculated for the system, with the goal of ensuring the temperature in the metallurgy does not exceed electromigration limits. Furthermore, the overall volume modelled is enlarged to evaluate the TCAD tools abilities to scale to larger and more complex models. The model, the methodology used and the results with specific attention to the scalability of the tools evaluated is discussed. The applicability of this methodology is demonstrated by showing the self-heating of measured structures is predicted with reasonable accuracy.

2:25 pm – 2:45 pm Paper Session B.4: Arvind Chokhani, Cadence
Title: Transition Delay Cell-Aware Test (Cadence)
Abstract: Cell-Aware Test (CAT) is a defect oriented test methodology which explicitly targets realistic defects inside technology library cells. Cell-aware ATPG targeting single-cycle static detects is fairly understood and matured. However, test generation for cell-internal defects requiring transition or two-pattern tests poses unique challenges. This paper proposes an untimed transition ATPG based approach to target such defects. Such an approach is found to be much more effective at generating test patterns than timed (delay) ATPG.

2:45 pm – 3:00 pm Paper Session B.5: Mike Lei, Marvell
Title: DFT ECO Verification with Logical Equivalence Formal Verification (Marvell)
Abstract: Logical Equivalence Formal Verification (LEFV) or Logical Equivalence check (LEC) has been used mainly in ASIC design to verify functional logic equivalence, not DFT logic equivalence. When a last-minute change is made to the DFT logic, what we call a DFT ECO, we need to verify it did not break any other DFT modes, such as the SIDESCAN or ASST modes. The usual method is to verify the DFT ECO through test structure verification (TSV) of the different test modes, such as using Cadence Modus TSV. However, due to the increasing design size, TSV runs can take days to weeks. Another method is to verify by gate level simulation, which may take even longer to run compared to TSV. It can be shown that the fastest way to verify the DFT ECO did not break any other DFT modes is to use LEFV. In summary, we can leverage LEFV to accelerate the verification of DFT ECOs. We were able to run LEFV on the 4 test modes in <30 hours, vs. days or weeks using TSV or gate level simulation verification.

Friday, May 21

10:00 am – 10:05 am Welcome: Eugene Atwood General Chair

Session 7

10:05 am – 11:10am Keynote Speaker Introduction: Danella Zhao

10:10 am – 11:10am Keynote speaker 7.1: **Hardware/Software Co-design for AI Systems**
Speaker: Prof. Yiran Chen, Duke Univ

Abstract: The rapid growth of modern neural network (NN) models' scale generates ever-increasing demands for high computing power of artificial intelligence (AI) systems. Many specialized computing devices have been also deployed in the AI systems,forming a truly application-driven heterogeneous computing platform. This talk discusses the importance of hardware/software co-design in AI system designs. We first use resistive memory based NN accelerators to illustrate the design philosophy of heterogeneousAI computing systems, and then present several hardware friendly efficient NN model design techniques. We also briefly introduce the automation of the co-design flow, e.g., neural architecture search. A research roadmap of our group in the relevant topicsis given at the end of the talk.

Biography: Yiran Chen received B.S (1998) and M.S. (2001) from Tsinghua University and Ph.D. (2005) from Purdue University. After five years in industry, he joined University of Pittsburgh in 2010 as Assistant Professor and then promoted to AssociateProfessor with tenure in 2014, held Bicentennial Alumni Faculty Fellow. He is now the Professor of the Department of Electrical and Computer Engineering at Duke University and serving as the director of NSF Industry–University Cooperative Research Center (IUCRC)for Alternative Sustainable and Intelligent Computing (ASIC) and the co-director of Duke Center for Computational Evolutionary Intelligence (CEI). His group focuses on the research of new memory and storage systems, machine learning and neuromorphic computing,and mobile computing systems. Dr. Chen has published 1 book and more than 400 technical publications and has been granted 96 US patents. He serves or served as the associate editor of more than ten international academic transactions/journals and served on the technical and organization committees of more than 60 international conferences. He is now serving as the Editor-in-Chief of the IEEE Circuits and Systems Magazine. He received seven best paper awards, one best poster award, and fourteen best paper nominations from international conferences and workshops. He is a distinguished lecturer of IEEE CEDA and listed in the HPCA Hall of Fame. He is a Fellow of the ACM and IEEE.

11:10 am – 11:15am Break

Paper Session C: Hardware Security

Session Chair: Martin Margala Session Co-chair: Malinky Ghosh

11:15 pm – 11:35 pm Paper Session C.1: Eric D Hunt-Schroeder, Univ. of Vermont
Title: Pre-Amplifier Based Entropy Source with Stable Output for use in a Physical Unclonable Function
Abstract: Physical Unclonable Functions (PUFs) produce full entropy keys without storing them. PUFs rely on a stable entropy source across voltage, temperature, and lifetime. Designed in GLOBALFOUNDRIES 14nm technology is a pre-amplifier based bitcell with >10x differential signal. A 1 Kb 2-d array includes a sense amplifier and current imbalance circuit to identify highly mismatched bitcells. Bits identified as highly mismatched are considered stable, solving one of the key challenges (repeatability) in developing a silicon based PUF.

11:35 pm – 11:55 pm Paper Session C.2: Bryan Moy, Stony Brook Univ.
Title: Low-Cost Encryption Core for Resource-Constrained Applications
Abstract: Resource-constrained systems such as Internet-of-things based devices have become increasingly more common. Each functionality within these systems needs to be optimized for power consumption. One such functionality is encryption to satisfy security and privacy concerns. A lightweight and low-cost SIMON cipher core was designed and manufactured in 0.5 µm CMOS technology targeting resource-constrained systems such as RFID applications and wireless sensors. The design employs a round-unrolled serial-to-parallel architecture to improve throughput while not compromising the benefits of low power consumption and area. The fabricated chip dissipates an average power of 1.03 mW during encryption while operating at the RFID frequency of 13.56 MHz, achieves an encryption efficiency of 3.29 Kb/sec/µW and consumes an area of 850 × 850 µm.

Noon – 1:00 pm Lunch

1:00 pm – 1:20 pm Paper Session C.3: Zhuoran Li , Old Dominion University
Title:A New Design of Smart Plug for Real-time IoT Malware Detection
Abstract: While Internet of Things (IoT) services are becoming pervasive, the cyber-attacks against IoT devices are in a sharp rise as well. Tailored for IoT devices, a low-cost, universal and real-time malware detection system is proposed that audits the side-channel power consumption data and extracts the distinguishable power features to detect malicious behaviors. In this paper, a new design of smart plug which is a core component of the system is designed, developed and prototyped to enable real-time power data collection, preprocessing and streaming for IoT malware detection. Our results demonstrate the promising performance of the smart plug in achieving real-time power auditing and high accurate malware detection.

Paper Session D: Papers: Micro Circuits & Microsystems Design and Emerging Technologies

Session Chair: Kelly Ockunzzi Session Co-chair: Nicola Nicolici

1:20 pm – 1:40 pm Paper Session D.1: Ruoyu Zhi, Green Mountain Semiconductor
Title: Opportunities and Limitations of in-Memory Multiply-and-Accumulate Arrays
Abstract: In-memory computing is a promising solution to solve the memory bottleneck problem which becomes increasingly unfavorable in modern machine learning systems. In this paper, we introduce an architecture of random access memory (RAM) incorporating deep learning inference abilities. Due to the digital nature of this design, the architecture can be applied to a variety of commercially available volatile and non-volatile memory technologies. We also introduce a multi-chip architecture to accommodate for varying network sizes and to maximize parallel computing ability. Moreover, we discuss the opportunities and limitations of in-memory computing as future neural networks scale, in terms of power, latency and performance. To do so, we applied this architecture to various prevalent neural networks, e.g. Artificial Neural Network (ANN), Convolutional Neural Network (CNN) and Transformer Network and compared the results.

1:40 pm – 2:00 pm Paper Session D.2: Yixuan He, Northeastern Univ.
Title: A Compensation Technique for Threshold Mismatch in Sub-threshold Current Mirror
Abstract: A novel compensation method is proposed to eliminate the threshold mismatch in sub-threshold current mirror. The gate voltage of the transistor pair in a basic current mirror is modified through a negative feedback loop during the tuning phase, thereby compensating the threshold variation from imperfect fabrication process. The circuit is implemented and simulated with 1.8V supply using standard 0.18μm CMOS technology and it accomplishes less than 1% inaccuracy with ±5% threshold variation in the 500nA input current range. The presented approach provides an accurate and continuous current copy in a wide current range while still preserving the original structure of the transistor pair, which means this technique can be implemented in various current mirror designs without affecting its input and output characteristics.

Break 2:00 pm - 2:05 pm

2:05 pm – 2:25 pm Paper Session D.3: Rasputha Rama Kanth Singi, Sree Vidyanikethan Engineering College, India
Title: High Performance Ternary Logic Gates Using GNRFET
Abstract: This research paper focuses on the design of GNRFET based inverters and universal gates in ternary logic. The ternary logic is considered to be better than two valued logic as it offers faster computations, reduced chip area, and smaller interconnects. Hence, it is possible to design in future integrated circuits with low-complexity, energy-efficient circuits and high-speed. A new approach is proposed for designing ternary logic circuits using graphene nanoribbon field-effect transistors (GNRFETs). In GNRFETs, the threshold voltage (Vth) is varied with the GNR width (W), described by the number of dimer lines (n).The various inverters such as standard, negative, and positive inverters are developed along with the NAND & NOR gates. The industry standard HSPICE simulator is used to simulate the proposed logic circuits for performance analysis and functional verification. Additionally, the performances of the proposed circuits are compared with the CNTFET based circuits. From the analysis, it is noticed that the GNRFET-based logic circuits show a performance improvement up to 32.6% over the CNTFET based circuits.

2:25 pm – 2:45 pm Paper Session D.4: Ernesto Sola-Thomas, Clarkson University
Title: Design of an Initial Prototype of the AI Wheelchair (Clarkson University)
Abstract: This paper presents the initial prototype of an AI wheelchair. It is a customized version of a commercially available manual wheelchair. The motivation of this research was to support individuals with limited

mobility in navigating their world. The proposed automated wheelchair consists of a stereo depth camera, LIDAR, DC gear motor, motor controller, joystick, emergency switch, processors, etc. The users have the option of controlling where their wheelchair goes by navigating themselves through the joystick or automatically through the developed hands-free application. This app relays back to the Jetson processor situated underneath the chair, which has the capability to move through any indoor location to reach the user's chosen destination. Although the initial research goal was to enable the wheelchair to navigate a patient through an indoor hospital facility, this low cost, lightweight wheelchair is envisioned to be employed in all indoor locations and accessible by a broader range of users than just the wealthy few. The project's design files have been made available so that this open-source wheelchair can be reproduced publicly.

2:45 am – 2:50am Invited Speaker Introduction: Danella Zhao

2:50 pm – 3:35 pm Invited Speaker 7.2: Hanhee Paik, Research Staff Member
IBM Quantum, IBM T J Watson Research Center, NY
Title: QUANTUM COMPUTING TECHNOLOGY: CHALLENGES AND FUTURE DIRECTIONS
Abstract: In the past decade, the quantum computing community has expanded from a small, research-focused group of physicists, engineers and mathematicians to a large interdisciplinary field that includes experts from all domains including industry, government, and academia. As a result, we have seen accelerated progress toward understanding the scope of quantum computing, advancing its hardware technology, and developing applications and error correction protocols. In this talk, I would like to present IBM's five-year vision for developing quantum computing technology, including how we will push the limits of hardware and how we make a quantum computer more practical by integrating with classical computing resources to increase execution capacity. At the end of the talk, I will briefly cover the directions and roles of materials science for quantum hardware development - what's the current limitation and what should be the future.
Biography: Dr. Hanhee Paik is a Research Staff Member at IBM Quantum, IBM T J Watson Research Center.
Through her research career, she has been focusing on understanding the coherence mechanisms of superconducting qubits and developing superconducting multi-qubit architectures. Dr. Paik pioneered the novel design of a superconducting qubit that helped the industry to push the boundary of superconducting qubit performance and her research on the quantum processor design has greatly impacted the quantum computing community. Today's IBM Quantum systems coherence times benefit from Dr. Paik's work, and average an industry-best 100microseconds. She played a pivotal role developing the 16-qubit IBM Q Experience device (Rueschlikon and Melbourne), and she is currently working on developing the next generation of quantum computing processors

3:35 pm – 3:40 pm Session 8.1: Symposium Wrap-up: Kelly Ockunzzi Vice General Chair

Announcement and dates for next year. May 16-18 2022
In person meeting planned with some virtual session content.