Nanotechnologies enabling future on-chip ESD protection

ESD failure is a major IC reliability problem. On-chip ESD protection is required for all ICs. As IC technologies and chip complexity continue to advance, on-chip ESD protection becomes more and more challenging. While R&D efforts have led to various advances, existing ESD protection structures and design techniques cannot meet the needs of ESD protection for future chips. Nanotechnologies open a door for future ESD protection exploration. This paper reviews a few emerging nanotechnology-based ESD protection concepts, including phase-changing nano crossbar array, graphene NEMS switch and graphene ESD interconnects, which have the potential to revolutionize future ESD protection designs.

Professor Albert Wang
Dept. of Electrical and Computer Engineering
University of California, Riverside, USA, aw@ece.ucr.edu

Biography: