2D Nanoelectronics Tutorial Session

As Moore's law approaches a physical limit, future semiconductor research requires high performance nanoelectronics (More Moore) and low-power and multifunctional devices (More than Moore). With the rise of graphene in 2004, two-dimensional (2D) van der Waals materials have attracted extensive attention and being considered one of the most promising material candidates for next-generation nanoelectronics, owing to ultrathin bodies, atomic smooth interfaces, passivated surfaces, good carrier mobility, and a sizable bandgap. These exceptional electronic properties in 2D materials with reduced dimensionality offer new opportunities to integrate with current Si technologies. In this special/tutorial session, we provide review and perspective of recent advances of 2D materials in nanoelectronics, and the topics cover from materials to devices and systems in both theories and experiments.

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2D Transistors: Promises, Problems and Prospects

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Two-dimensional (2D) semiconductors have attracted tremendous interest as an atomically thin channel for the continued transistor scaling. However, despite many proof-of-concept demonstrations, the full potential of 2D transistors remains elusive. To this end, the fundamental merits and technological limits of 2D transistors need a critical assessment, reality check and objective projection. In this talk, I will briefly review the promises and the current status of 2D transistors, and highlight the widely used device parameters (e.g., carrier mobility, contact resistance) could be frequently misestimated or misinterpreted, and may not be the most reliable performance metrics for benchmarking 2D transistors. We suggest the saturation or on-state current density, especially in the short channel limit, could provide a more reliable measure for assessing the potential of diverse 2D semiconductors, and should be applied for cross-checking different studies, especially when milestone performance metrics are claimed. We next summarize the key technical challenges in optimizing the channel, contacts, dielectric and substrate interfaces and outline the potential pathways to push the limit of 2D transistors; and lastly conclude with a prospect on the critical technical targets, the key technological hurdles to enable the lab-to-fab transition, and the potential opportunities arising in these atomically thin semiconductors.

Bio: Dr. Duan received his B.S. Degree from University of Science and Technology of China in 1997, and Ph.D. degree from Harvard University in 2002. He was a Founding Scientist and then Manager of Advanced Technology at Nanosys Inc., a nanotechnology startup founded based partly on his doctoral research. Dr. Duan joined UCLA with a Howard Reiss Career Development Chair in 2008, and was promoted to Associate Professor in 2012 and Full Professor in 2013. Dr. Duan's research interest includes nanoscale materials, devices and their applications in future electronic and energy technologies. Dr. Duan has published over 300 papers with nearly 80,000 citations, and holds 52 issued US patents. Dr. Duan has received many awards for his pioneering research in nanoscale science and technology, including MIT Technology Review Top-100 Innovator Award, NIH Director's New Innovator Award, NSF Career Award, Alpha Chi Sigma Glen T. Seaborg Award, Herbert Newby McCoy Research Award, US Presidential Early Career Award for Scientists and Engineers (PECASE), ONR Young Investigator Award, DOE Early Career Scientist Award, Human Frontier Science Program Young Investigator Award, DuPont Young Professor, Journal of Materials Chemistry Lectureship, International Union of Materials Research Society and Singapore Materials Research Society Young Researcher Award, the Bellby Medal and Prize, the Nano Korea Award, International Society of Electrochemistry Zhao-Wu Tian Prize for Energy Electrochemistry, Science China Materials Innovation Award, AIP Horizons Lectureship and Materials Research Society Middle Career Award. He is currently an elected Fellow of Royal Society of Chemistry and Fellow of American Association for the Advancement of Science.

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2D Nanoelectronics: New Materials and Devices for Edge Intelligence

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The end of traditional transistor scaling brings unprecedented new opportunities to semiconductor devices and electronics. We are at the onset of a new technology revolution, which will focus on distributed intelligence and will be pushing the limits of sensing and computing at the edge of the cloud. Silicon chips alone are not enough to deliver the performance needed by future systems. We need co-integration of new materials with Silicon to deliver both quantitative and qualitative performance boosters to the silicon chips.

Two dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDs) will be key enablers of this new generation of electronics. In this talk, we will describe some of our work to integrate both graphene and TMDs into electronic systems with unique performance and functionality. Some of the topics to be covered include 1. High performance MoS2 transistors and circuits for integration at the back-end-of-the-line of Silicon technology; 2. New optical and wi-fi energy harvesters to enable ubiquitous electronics; and 3. A new generation of cell-sized autonomous electronic microsystems to revolutionize invisible sensing. The talk will conclude with a reflection on how design-technology co-optimization (DTCO) is critical for developing functional systems based on new materials with yields and uniformity levels very different from the ones typically found in traditional silicon electronics. When combining DTCO, with the democratization of heterogeneous integration, the unique properties of extreme materials and the opportunities of distributed intelligence will transform our society just as Moore's law has done for the last 50 years.

Bio: Tomás Palacios is a Professor in the Department of Electrical Engineering and Computer Science at MIT. He received his PhD from the University of California - Santa Barbara in 2006, and his undergraduate degree in Telecommunication Engineering from the Universidad Politecnica de Madrid (Spain). His current research focuses on demonstrating new electronic devices and applications for novel semiconductor materials such as graphene and gallium nitride. His work has been recognized with multiple awards including the Presidential Early Career Award for Scientists and Engineers, the 2012 and 2019 IEEE George Smith Award, and the NSF, ONR, and DARPA Young Faculty Awards, among many others. Prof. Palacios is the founder and director of the MIT MTL Center for Graphene Devices and 2D Systems, as well as the Chief Advisor and co-founder of Cambridge Electronics, Inc. He is a Fellow of IEEE.

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Sensing, Computing, Storage, and Hardware Security Devices Based on 2D Materials

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My group is developing a new paradigm of sensing, computing, storage, and hardware security inspired by the neurobiological architectures and neural algorithms found inside various animal brains that allow evolutionary success in resource constrained environments. Towards the realization of our vision, we exploit unique electronic and optoelectronic properties of layered two dimensional (2D) materials such as graphene, MoS\textsubscript{2}, WSe\textsubscript{2}, black phosphorous etc., to design high performance, ultra-low-power, artificially intelligent, and inherently secure solid state devices inspired by natural intelligence. For example, we have mimicked auditory information processing in barn owl (Nature Communications, 10, 3450, 2019), collision avoidance by locust (Nature Electronics, 3, 646-655, 2020), and subthreshold signal detection by paddlefish and cricket using stochastic resonance (Nature Communications, 2020). We have also mimicked probabilistic computing in animal brains using low-power Gaussian synapses (Nature Communications, 10, 4199, 2019), and memristive graphene synapses (Nature Communications, 11, 5474, 2020) and realized biomimetic devices that can emulate neurotransmitter release in chemical synapses (ACS Nano, 11, 3, 2017) and neural encoding in afferent neurons (Nature Communications, 12, 2143, 2021). We have also made these device secure through SAT-attack resistant hardware obfuscation using camouflaged 2D heterostructures (ACS Nano, 15, 2, 2021) and by realizing machine learning resilient and reconfigurable physically unclonable functions (Nature Electronics 4, 364-374, 2021).

Bio: Dr. Das received his B.Eng. degree (2007) in Electronics and Telecommunication Engineering from Jadavpur University, India, and Ph.D. degree (2013) in Electrical and Computer Engineering from Purdue University. He was a Postdoctoral Research Scholar (2013-2015) and Assistant Research Scientist (2015-2016) at Argonne National Laboratory (ANL). Dr. Das joined the Department of Engineering Science and Mechanics (ESM) at Penn State University in January 2016. Dr. Das was the recipient of Young Investigator Award from United States Air Force Office of Scientific Research in 2017 and National Science Foundation (NSF) CAREER award in 2021. Das Research Group at Penn State leads a new multidisciplinary area of science, namely biomimetic sensing, neuromorphic computing, and hardware security inspired by natural designs found in the animal world that allow evolutionary success in resource-constrained environments.

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