31st IEEE Microelectronics Design & Test Symposium 2022

The 31st IEEE Microelectronics Design & Test Symposium (MDTS), formerly known as the North Atlantic Test Workshop (NATW) was held this year as four live Zoom meeting sessions on May 23rd through May 26th. Travel restrictions caused by the Covid-19 pandemic caused us to adapt from a face-to-face meeting to a virtual symposium. The symposium continues to provide a forum for discussion of current and future issues in VLSI design. The symposium encourages original research and work-in-progress submissions from any area encompassed by topics in high quality design for test techniques and methodologies. The MDTS theme this year was "*Innovation in Microelectronics for AI, Security, and New Advances in Computing.*" A theme intended to provoke symposium participants to explore modern technologies in AI and Security. The two symposium sessions included presentation of twenty peer reviewed research papers, three invited speakers, three tutorials and a panel discussion.

The May 23rd tutorial session was chaired by Krishna Chakravadhanula and Huamin Li and began with a tutorial session by Xiangfeng Duan, University of California, Los Angeles, titled "2D Transistors: Promises, Problems and Prospects". The focus of this talk was the status of 2D transistors, device parameters, and highlighted the widely used device parameters and technological hurdles. This was followed by a tutorial by Tomás Palacios, Massachusetts Institute of Technology, discussing "2D Nanoelectronics: New Materials and Devices for Edge Intelligence". This tutorial discussed methodologies to integrate both graphene and TMDs into electronic systems to improve performance and functionality. The last tutorial was given by Saptarshi Das, Pennsylvania State University on "Sensing, Computing, Storage, and Hardware Security Devices based on Two-dimensional (2D) Materials". This tutorial explained electronic and optoelectronic properties of layered two dimensional (2D) materials such as graphene, MoS2, WSe2, black phosphorous etc., to design high performance, ultra-low-power, artificially intelligent, and secure solid-state devices inspired by natural intelligence. The day ended with a Keynote presentation on "Industry Trends as Globalized Supply Chains Restructure" by Joseph Fitzgerald, Deloitte Consulting LLC and Garrett Wyatt, Siemens Digital Industries Software.

The May 24th Invited Speaker session was organized and chaired by Kelly Ockunzzi, General Chair and Eugene Atwood, IBM. "On-chip analysis of fluid flow for applications in carbon dioxide trapping" was discussed by Jaione Tirapu Azpiroz, IBM. Key elements in this speech include the progress in the development of microscopy and spectroscopy techniques that can be applied on-chip to monitor the flow of CO2-laden fluids in constricted geometries. This was followed by Student Paper Session 1a chaired by Uma Srinivasan, IBM where 3 peer reviewed papers were presented - 'Ge/GaAs Hetero-structured n-p-n Transistor' by Dhawal N Asthana, UMass Lowell, "Autonomous Navigation System from Simultaneous Localization and Mapping" by Micheal Caracciolo, Clarkson University, and "Enhanced DFT for Fortuitous Detection of Transition Faults During Scan Shift" by

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Hui Jiang, Southern Methodist University. Student Paper Session 1b was chaired by Brion Keller, and covered 3 more peer reviewed papers - "Modeling and Design of Low Threshold Voltage D-mode GaN HEMT" by Dhawal N Asthana, Umass Lowell, "Impact of Switching Variability, Memory Window, and Temperature on Vector Matrix Operations Using 65nm CMOS Integrated Hafnium Dioxide-based ReRAM Devices" by Maximilian Liehr, College of Nanoscale Science & Engineering SUNY Polytechnic Institute, and "27/38 GHz Dual-Band Subsampling PLL Design with Automated Frequency Calibration" by Wenzhe Chen, University of Vermont. The last paper session of the day was chaired by Eugene Atwood and went through the peer reviewed papers - "Design and Testing Considerations for a Multi-State Magnetic Memory Device" by Wolfgang Hokenmaier, Green Mountain Semiconductor, Inc, "Wide Range Variable Capacitance Controlled by Electrostatic MEMs" by Sam Mil'shtein, UMass Lowell and "iBUG: AI Enabled IoT Sensing Platform for Real-time Environmental Monitoring" by Md Faishal Yousuf, University of New Hampshire.

Wednesday May25th session started with Invited Speaker Albert Wang, University of California, Riverside discussing "Nanotechnologies enabling future on-chip ESD protection". This was followed by the Panel discussion chaired by Malinky Ghosh, IBM, on "Closing the Collaboration Gap Between Industry and Academia." Paper sessions in the afternoon were chaired by Paul Reuter on the following topics - "Big chips, abutted designs, and DFT" by Kevin Gorman, ASIC Central Engineering, Marvell Technology, Inc., "A novel framework for checking and automating DRC Rules" by Jiseong Kim, Samsung, "Detecting Temporal Correlation on HfO2 Based RRAM on 65nm CMOS Technology" by Sarah Rafiq, College of Nanoscale Science and Engineering, SUNY Polytechnic Institute, "Design of a simple SARS-CoV-2 (COVID-19) detector for fast detection" by Supriya Karmakar, Farmingdale State College-SUNY, and "Fault Coverage Analysis using Sneak Path based Testing in Memristor Circuits" by Rasika Joshi, Intel Corporation.

The final day of the Conference started on Thursday May 26th, with Invited speakers, Lakshmanan Balasubramanian, Supraja R, and Rubin Parekhji, Texas Instruments Pvt. Ltd., India reviewing "Applications of Analog Defect Simulation to Digital, Memory, ADC and Package Level Tests". This was followed by paper sessions chaired by Tian Xia and covered many topics - "Detection and Classification of PCB Defects using Deep Learning Methods" by Andria Legon, Dept. of Computational Modeling and Simulation Engineering, Old Dominion University, "Fast Turn Around Time Development Flow for high Quality LVS rule files" by Ahmed Saleh, Siemens EDA, "In 12nm FinFET Technology, performance analysis of low power 6T SRAM layout designs with two different topologies" by Sajib Barua, Circuit and System Design Department, Ulkasemi Private Limited, "Multi-Heuristic Machine Intelligence Guidance in Automatic Test Pattern Generation" by Soham Roy, Intel Corporation, "Design of Ballistic MOSFET for Operation at Terahertz Frequencies" by Samson Mil'shtein, Umass Lowell, and "Fast and Accurate post-layout simulation

methodology using 4nm LVS rule deck" by Woonggyu Lee, Samsung. Closing Remarks and Best Student Paper Award were delivered by Vice General Chair, Andrew Laidler. Maximilian Liehr was awarded Best Paper award for his student paper on "Impact of Switching Variability, Memory Window, and Temperature on Vector Matrix Operations Using 65nm CMOS Integrated Hafnium Dioxide-based ReRAM Devices".

The symposium technical papers program is available in the IEEE Explore Digital Library and can be located using the search term **"31st Microelectronics Design and Test Symposium".** MDTS also has made the proceedings, including tutorial presentations, available to registered attendees.

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