Call for Papers

The 32nd Microelectronics Design & Test Symposium (IEEE MDTS 2023)

(Tentative) May 8 – 10, 2023

Albany, New York

http://mdts.ieee.org

Key Dates

Submission Due Date:
2023/02/26
Acceptance Notification Date:
2023/04/07
Final Paper Submission Date:
2023/04/30

Organizing Committee

General Chair
Kelly Ockunzzi – Marvell
Vice General Chair
Andy Laidler – onsemi
Program Chair
Uma Srinivasan – IBM
Vice Program Chair
Huamin Li – Univ. at Buffalo
Past General Chair
Eugene Atwood – IBM
Tutorial Co-Chairs
Carl Wisnesky – Cadence
Krishna Chakravadhanula – Cadence
Special Session Chair
Kevin Gorman – Marvell
Panel Chair
Malinky Ghosh – IBM
Finance & Registration
Charles Thangaraj – Univ. of St. Thomas
Ryan Patterson – CACI
Xinghao Chen – IEEE
Ted Cooley – Cooley & Company
Publication Chair
Themistoklis Haniotakis – S. Illinois Univ.
Vice Publication Chair
Tian Xia – Univ. of Vermont
Publicity Chair
Eric Hunt-Schroeder – Marvell
Web Master
Yu Zhang – Aptiv

Steering Committee

Vishwani Agrawal – Auburn Univ.
Xinghao Chen – IEEE
Ted Cooley – Cooley & Company
Jennifer Dworak – SMU
Brion Keller – Lockheed Martin
Karen Panetta – Tufts University
Paul Reuter – Siemens EDA
Peilin Song – IBM Research
Tian Xia – Univ. of Vermont
Krishnat Patil – IEEE Schenectady
Charles Rubenstein – Pratt Institute

Sponsors

IEEE Region 01 – Northeastern USA
IEEE Schenectady Section

Contact

Uma Srinivasan, Program Chair
umasrin@us.ibm.com
Kelly Ockunzzi, General Chair
kockunzzi@marvell.com

Theme

Artificial Intelligence, Machine Learning, and Deep Learning: Tactical and Strategic Impacts to Microelectronics Design and Test

The IEEE Microelectronics Design & Test Symposium (MDTS) provides a forum for academic and industry researchers and engineers to discuss the latest advances in microelectronics, share their visions in modern microelectronic technologies, and foster academic-industry collaboration. The 32nd MDTS features artificial intelligence (AI), machine learning (ML), and deep learning (DL). AI/ML/DL algorithms can be used to improve design and test by evaluating the accuracy and effectiveness of models, design rules, and test coverage. In addition, new circuits and chip architectures for AI/ML/DL applications are emerging, presenting new challenges to design and test in the form of reticle-size die, chiplets, and hardware/software co-design.

Topics of interest include but are not limited to:

Micro Devices, Circuits and Microsystems: Analog/mixed-signal/radio frequency (RF) circuits; Low-power low-voltage design; Sensors and sensing systems; Smart system design for automotive, automation and robotics; Circuits and systems for approximate and evolvable computing; Memristor-based devices; Lab-on-Chip, wearable and implantable devices; Heterogeneous integration and multi-scale chiplet-based packaging architecture

Biomedical, Photonics, and Quantum Electronics: Biomedical and bio-inspired circuits and systems; Microelectromechanical systems (MEMS) sensors and bioelectronics; Nanobiophotonics for optical imaging, sensing, and diagnostics; Terahertz photonics for communications; Photodetectors, sensors, and imaging; Photonics for energy and green photonics

Electronic Design & Test Methodologies and Electronic Design Automation (EDA): Electronic design tools, processes and methodologies; EDA for 3D integrations and advanced packaging; EDA for bio-inspired and neuromorphic systems; EDA tools, methodologies and applications for Photonics devices, circuit, and system design; System-on-Chip (SoC)/intellectual property (IP) testing strategies; Hardware/software co-verification; Design for testability (DFT) & built-in self-test (BIST) for digital designs, analog/mixed-signal integrated circuits (ICs), SoCs, and memories; Design verification/validation; Machine learning datasets for microelectronics design and test

Hardware Security: Microarchitectural attacks; Side channel attacks and mitigation; (Anti-)Reverse engineering and physical attacks; Hardware obfuscation; Computer-aided design (CAD) for security; SoC security, Field-programmable gate array (FPGA) and reconfigurable fabric security; Internet-of-Things (IoTs) and cyber physical system security

Emerging Technologies and Applications: Computing-in-memory architectures; Neural networks, AI, ML, and DL in design and test of microelectronics; IoT, edge nodes, or pipelines for real-time data visualizations and monitoring in design and test of microelectronics; Application of cognitive, neuromorphic and quantum computing; High-speed serializer/deserializer (SerDes); Next-generation design-technology co-optimization; Advanced interconnect; 3D manufacturing

The Program Committee invites researchers and practitioners to submit tutorial, panel, and special session proposals related to the theme. Proposals must include title, topic abstract, speakers' short bio, and a list of contributing papers. The committee also encourages authors to submit original, unpublished papers on any of the topics of interest. Submissions may be six-page full papers or two-page extended summaries. Accepted papers presented at the symposium have the option of being published in IEEE *Xplore*®. Full details can be found on the **mdts.ieee.org** website.

Jake Karrfalt Best Student Paper Award

To encourage student participation in the microelectronics research community, MDTS will recognize the top student first-author paper and presentation.

2022 Corporate Supporters

SIEMENS IBM ADVANTEST AdamsIP.com Patenting for Software & Electronics SWTEST cadence onsemi