32nd IEEE Microelectronics Design & Test Symposium 2023

The 32nd IEEE Microelectronics Design & Test Symposium (MDTS), formerly known as the North Atlantic Test Workshop was held this year at the Crowne Plaza Desmond Hotel, Albany, New York, USA, from May 8th through May 10th. We successfully transitioned to a traditional in-person format for the symposium, from the virtual symposiums held during the Covid-19 pandemic. The symposium continues to supply a forum for discussion of current and future issues in VLSI design while encouraging original research and work-in-progress submissions from any area encompassed by topics in high quality design for test techniques and methodologies. The MDTS theme this year was "*Artificial Intelligence, Machine Learning, and Deep Learning: Tactical and Strategic Impacts to Microelectronics Design and Test.*" - a theme intended to provoke symposium participants to explore modern technologies in AI and ML. The three-day symposium sessions included presentation of fifteen peer reviewed research papers, two keynote speeches, five invited speakers, two tutorials and a panel discussion "*Make No Mistake AI: Discussions on how we use Machine Learning and Artificial Intelligence Results*".

The Symposium started on Monday May 8th in the afternoon with a Welcome Address by our General Chair, Kelly Ockunzzi. The welcome address was followed by Invited Speaker Qiaoyan Yu, Professor at the Department of ECE at University of New Hampshire, presentation on *"Hardware Security in The Era of Machine Learning"*. It was an engaging and interactive talk focused on training with machine learning to distinguish between real defects in hardware versus malicious attacks. The invited speaker was followed by a Keynote presentation *"IBM Telum: real-time AI for enterprise applications"* given by Christian Jacobi, IBM Fellow, System Architecture & Design, System Z. Christian discussed the concept of Hybrid Cloud and the balance of latency versus workload versus number of cores. Next a tutorial by Rob Aitken, Distinguished Architect, Office of Technology Strategy at Synopsys on *"Implications of AI on Microelectronics Design and Test".* Rob highlighted the use of Neural Networks and Machine Learning in a case study for image processing using a raspberry pi video monitor. The day ended with a panel discussion on *"Make No Mistake AI: Discussions on how we use Machine Learning and Artificial Intelligence Results"* with panelists – IBM Fellow, Christian Jacobi, VP of Technology at Marvell Semiconductors, Mark Kuemerle, and Director of Federal Strategy at Intel Federal, Shawn Fetterolf. The panel was chaired by Malinky Ghosh and moderated by Eugene Atwood. Shawn's presentation on "AI/ML Innovation and Impacts on Chip Design" kicked off the discussion, going over the semiconductor and packaging landscape today and how it is changing as we introduce AI/ML to do verification, large scale deployment and saves design, verification, and software costs. Some of the panelist responses to questions reiterated the importance of the input going into an AI tool such as Chat GPT and who manages confirming this data. The question of data volume involved and complexity, as well as impacts of input tampering, supplied interesting discussion points. The rallying point of the panel discussion was about the trustworthiness of this modern technology, and intriguing ideas on whether it replaces jobs or helps us offload monotonous workload, in the end allowing more time for innovation. The

other aspects of this interactive session delved into questions of ethics of patenting the IP generated with AI tools and originality of code or other works generated by AI. The conclusion was that we must wait to see this accelerating pace of growth in AI and ML and learn as we grow with it, to apply this technology effectively.

On May 9th, we started the day with the Invited Speaker, Mark Kuemerle, VP of Technology for Marvell's Compute and Custom Business, talking about *"Machine learning madness: achieving performance in an era of reduced scaling and extraordinary costs.".* Key elements in this speech addressed scaling limits in chip design and using ML in the architecture and floor planning for chips driving solutions that improve area scaling while optimizing wire lengths and power. This was followed by Student Paper Session 1, chaired by Krishna Chakravadhanula, Cadence, where five peer reviewed papers were presented – "A Machine Learning Approach for Person Authentication from EEG Signals" by A M Mahmud Chowdhury, Clarkson University; "A Supervised Deep Learning Method for Designing A Series-Fed Microstrip Array Antenna" by Yan Zhang, University of Vermont; "Regression Models to Predict Memory Usage of High-Cost Analysis Jobs" by Brandon Ung, University of Minnesota Twin Cities; "Analog NVM Synapse for Hardware-Aware Neural Network Training Optimization on 65nm CMOS TaOx ReRAM Devices" by Maximilian Liehr, SUNY Polytechnic Institute; and "Reconfigurable Self-Destructing Pre-Amplifier Physical Unclonable Function" by Eric Hunt-Schroeder, University of Vermont.

The Tuesday afternoon session started with a Keynote speech by Azalia Mirhoseini, Member of Technical Staff at Anthropic and Assistant Professor at Stanford, on *"Pushing the Limits of Scaling Laws in the Age of Large Language Models*". Azalia talked about how AI can improve scaling by innovating across data, models, software, and hardware. She illustrated the use of reinforcement learning from human and AI feedback to improve learning efficiency and parameter efficiency, an automated framework for co-designing AI accelerators, and a deep Reinforcement Learning (RL) method for chip floor planning used in multiple generations of Google AI's accelerator chips (TPU). The keynote was followed by Student Paper Session 2, chaired by Andrew Laidler, onsemi, on the following topics - "Effects of Processing Variables on Tantalum Oxide Resistive Random Resistive Random Access Memory (ReRAM) Performance" by Rajas Mathkari, SUNY Polytechnic Institute; "Flow-Based Computing of NOR Logic Using ReRAM Devices" by Zachery Woods, SUNY Polytechnic Institute; and "Effect of Resistance variability in Vector Matrix Multiplication operations of 1T1R ReRAM crossbar arrays using an Embedded test platform " by Jeelka Solanki, SUNY Polytechnic Institute. The final talks on day two were given by two invited speakers - Reza Zadeh, Adjunct Professor at Stanford University and CEO of Matroid on the topic "Attacking Computer Vision", followed by Rob Knoth, Group Director in Cadence's Digital & Signoff Group, on "Delivering on the Promise of AI/ML SoC Design". Reza talked about the challenges in using computer vision in sensitive systems and the security issues in production systems. Rob Knoth touched on the application of generative AI to system designs resulting in better convergence backed

by Cadence's silicon products to address SoC design challenges. The day ended with a Banquet Dinner and presentation of Best Student Paper Award by Andrew Laidler, to Jeelka Solanki for her paper titled "Effect of Resistance variability in Vector Matrix Multiplication operations of 1T1R ReRAM crossbar arrays using an Embedded test platform."

Wednesday May 10th, the final day of the Conference, started with Paper Session 3, chaired by Professor Tian Xia from University of Vermont. This Paper Session comprised three peer reviewed papers from the industry - "RF Wireless Chatting" in short format by Supriyo Karmakar, SUNY Farmingdale College; "A Subject-Independent Machine Learning Model to Recognize Hand Gestures from Surface Electromyography Signals" by Sean Furman, Associate Engineer, Andro Computational Solutions; and "Autonomous Object Tracking Drone" in short format by Supriyo Karmakar, SUNY Farmingdale College.

The last Paper Session, 4, was chaired by Eric Hunt-Schroeder from Marvell Semiconductor Inc. and included four peer reviewed papers - "Application of machine learning methods for the diagnosis of Lyme disease with a fluorescent plasmonic biosensor" by Benjamin Taubner, SUNY Polytechnic Institute; "Time-Frequency Deep Learning Classification Model for Differentiating Metal Oxide Coated Particles For Bioelectronic Applications" by Umer Hassan, Assistant Professor of ECE, Rutgers University; "Application of Artificial Intelligence (AI) in Yield Analysis and Fault Isolation in Semiconductor Processing" by Supriyo Karmakar, SUNY Farmingdale College; and "A Real Time FPGA-based IQ Imbalance Measurement and Calibration System for High Volume Production Testing" by Xiaozhe Fan, GlobalFoundries. The symposium ended with the closing remarks delivered by Vice General Chair, Andrew Laidler.

The symposium technical papers program will be available in the IEEE Explore Digital Library in the next few weeks and can be found using the search term **"32nd Microelectronics Design and Test Symposium".** MDTS also has made the proceedings, including tutorial presentations, available to registered attendees.

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