Call for Participation

The 33rd Microelectronics Design & Test Symposium (IEEE MDTS 2024)

May 13 – 15, 2024

Crowne Plaza Albany - The Desmond Hotel in Albany, New York

http://mdts.ieee.org

Key Dates

Full Paper or Extended Summary:
02/22/2024
Notification of Acceptance:
04/01/2024
Final Paper Submission:
05/01/2024

Organizing Committee

General Chair
Kelly Ockunzzi – Marvell
Vice General Chair
Andy Laidler – onsemi
Program Chair
Uma Srinivasan – IBM
Vice Program Chair
Huamin Li – Univ. at Buffalo
Past General Chair
Eugene Atwood – IBM
Tutorial Co-Chairs
Carl Wisnesky – Cadence
Krishna Chakravadhanula – Cadence
Special Session Chair
Qiaoyan Yu (Univ. of New Hampshire)
Nathaniel Cady (Univ. at Albany)
Panel Chair
Malinky Ghosh – IBM
Finance & Registration
Charles Thangaraj – Univ. of St. Thomas
Ryan Patterson – CACI
Xinghao Chen – IEEE
Ted Cooley – Cooley & Company
Publication Chair
Themistoklis Haniotakis – S. Illinois Univ.
Vice Publication Chair
Tian Xia – Univ. of Vermont
Publicity Chair
Eric Hunt-Schroeder – Marvell
Web Master
Yu Zhang – Aptiv

Steering Committee

Vishwani Agrawal – Auburn Univ.
Xinghao Chen – IEEE
Ted Cooley – Cooley & Company
Jennifer Dworak – SMU
Brion Keller – Lockheed Martin
Karen Panetta – Tufts University
Paul Reuter – Siemens EDA
Peilin Song – IBM Research
Tian Xia – Univ. of Vermont
Krishnat Patil – IEEE Schenectady
Charles Rubenstein – Pratt Institute
Eugene Atwood – IBM

Contact

Uma Srinivasan, Program Chair
umasrin@us.ibm.com
Kelly Ockunzzi, General Chair
kockunzzi@marvell.com

Theme
Advances and Challenges for Chiplets and for Hardware Security

The IEEE Microelectronics Design & Test Symposium (MDTS) provides a forum for academic and industry researchers and engineers to discuss the latest advances in microelectronics, share their visions in modern microelectronic technologies, and foster academic-industry collaboration. The 33rd MDTS explores challenges and advances on two major fronts: chiplets and hardware security. Chiplets break large chip designs into smaller, ideally reusable, blocks, and the Universal Chiplet Interconnect Express (UCIe) standard addresses the challenges of connecting chiplets in the package. Hardware security for chip designs covers a broad range of issues, from preventing reverse engineering to blocking takeovers and data theft or manipulation. Topics of interest include but are not limited to:

Micro Devices, Circuits and Microsystems: Analog/mixed-signal/radio frequency (RF) circuits; Low-power low-voltage design; Sensors and sensing systems; Smart system design for automotive, automation and robotics; Circuits and systems for approximate and evolvable computing; Memristor-based devices; Lab-on-Chip, wearable and implantable devices; Heterogeneous integration and multi-scale chiplet-based packaging architecture

Biomedical, Photonics, and Quantum Electronics: Biomedical and bio-inspired circuits and systems; Microelectromechanical systems (MEMS) sensors and bioelectronics; Nanobiophotonics for optical imaging, sensing, and diagnostics; Terahertz photonics for communications; Photodetectors, sensors, and imaging; Photonics for energy and green photonics

Electronic Design & Test Methodologies and Electronic Design Automation (EDA): Electronic design tools, processes and methodologies; EDA for 3D integrations and advanced packaging; EDA for bio-inspired and neuromorphic systems; EDA tools, methodologies and applications for Photonics devices, circuit, and system design; System-on-Chip (SoC)/intellectual property (IP) testing strategies; Hardware/software co-verification; Design for testability (DFT) & built-in self-test (BIST) for digital designs, analog/mixed-signal integrated circuits (ICs), SoCs, and memories; Design verification/validation; Machine learning datasets for microelectronics design and test

Hardware Security: Microarchitectural attacks; Side channel attacks and mitigation; (Anti-)Reverse engineering and physical attacks; Hardware obfuscation; Computer-aided design (CAD) for security; SoC security, Field-programmable gate array (FPGA) and reconfigurable fabric security; Internet-of-Things (IoTs) and cyber physical system security

Emerging Technologies and Applications: Computing-in-memory architectures; Neural networks, AI, ML, and DL in design and test of microelectronics; IoT, edge nodes, or pipelines for real-time data visualizations and monitoring in design and test of microelectronics; Application of cognitive, neuromorphic and quantum computing; High-speed serializer/deserializer (SerDes); Next-generation design-technology co-optimization; Advanced interconnect; 3D manufacturing

The Program Committee invites researchers and practitioners to submit tutorial, panel, and special session proposals related to the theme. Proposals must include title, topic abstract, speakers' short bio, and a list of contributing papers. The committee also encourages authors to submit original, unpublished papers on any of the topics of interest. Submissions may be six-page full papers or two-page extended summaries. Accepted papers presented at the symposium have the option of being published in IEEE *Xplore*®. Full details can be found on the **mdts.ieee.org** website.

Jake Karrfalt Best Student Paper Award

To encourage student participation in the microelectronics research community, MDTS will recognize the top student first-author paper and presentation.

2023 Sponsors and Corporate Supporters

IEEE Region 01 – Northeastern USA

IEEE Schenectady Section

SIEMENS IBM IEEE young professionals ADVANTEST AdamsIP.com Patenting for Software & Electronics SWTEST cadence onsemi

Call for Participation

The 33rd Microelectronics Design & Test Symposium (IEEE MDTS 2024)

May 13 – 15, 2024

Crowne Plaza Albany - The Desmond Hotel in Albany, New York

http://mdts.ieee.org

Invited Talks and Tutorials

Scan Chain Attacks on AI Hardware

Seetal Potluri, Assistant Professor
Department of Electrical and Computer Engineering
University at Albany

Emerging Security Challenges at the Junction of AI and Hardware

Aydin Aysu, Assistant Professor
Department of Electrical and Computer Engineering
NC State University

NIST-SRC Microelectronic and Advanced Packaging Roadmap

John Oakley, Science Director
Semiconductor Research Corporation

Everything You Always Wanted to Know about UCIe

Martin Cochet, Senior Research Scientist
IBM Research

IEEE P3405 Introduction, Status Update (Chiplet Interconnect Test and Repair)

Paul Reuter, Senior Software Engineer
Siemens Digital Industries Software

On the Dark Side of FPGA as A Cloud-Hardware Accelerator

Xiaolin Xu, Assistant Professor
Department of Electrical and Computer Engineering
Northeastern University

Chiplets for Security and Security for Chiplets

Ramesh Karri, Professor
Department of Electrical and Computer Engineering
New York University

Side-channel Leakage in Superconducting Electronics: Foe or Friend?

Selçuk Köse, Associate Professor
Department of Electrical and Computer Engineering
University of Rochester

Panel Discussion

Rise of the Chiplets - Design, Test and Hardware Security

Chiplets are increasingly becoming the new frontier where they may provide an avenue to enable the continuation of Moore's Law not on a single monolithic die but by building functionality on multiple dies and integrating those within a package. This can potentially help to increase yield, make systems more modular so that they don't all have to be redesigned at the same time, allow the best fabrication technology to be used for each piece of the system and even perhaps in the future to reduce total system cost and enable chiplets to be purchased in a third-party market. As the possibilities are endless, the leading-edge companies are beginning to establish the course for the industry, and standards are being put in place. However, there are several hurdles and problems that need to be resolved before chiplet technology becomes a mainstream technology. This panel seeks to shed light on where the industry is at regarding adoption of chiplets, barriers to implementation and scalability, security issues, roadmaps currently in place, return on investment and much more.

Host
Eugene Atwood
Advisory Engineer / Research Scientist
IBM

Panelist
Ramesh Karri
Professor, Electrical and Computer Engineering
New York University

Martin Cochet
Senior Research Scientist
IBM Research

Nathaniel Cady
Associate Dean
University at Albany, The State University of New York

Paul Reuter
Senior Software Engineer
Siemens Digital Industries Software

Student and Young Professional Forum

A dedicated forum for students and young professionals will be arranged during the symposium. Further details will be announced soon.

Tour: Albany Nanotech Complex

The Albany NanoTech Complex is home to the College of Nanoscale Science and Engineering, the University at Albany. The site offers a fully-integrated research, development, prototyping, and educational facility that provides strategic support through outreach, technology acceleration, business incubation, pilot prototyping, and test-based integration support for onsite corporate partners including IBM, GlobalFoundries, Samsung, Applied Materials, Tokyo Electron, ASML and Lam Research, as well as other “next generation” nanotechnology research activities, including hands-on internships for students along with career opportunities. The Complex includes the Zero Energy Nanotechnology (ZEN) building, NanoFab Xtension, East, North, South, and 200 (also know as CESTM). In sum, the 1.65 million square-foot NanoTech megaplex boasts billions of dollars in high-tech investments and hundreds of corporate partners since its inception, with thousands of R&D jobs on site. Further details will be announced soon.

Source: SUNY Polytechnic Institute