

2024 IEEE Microelectronics Design and Test Symposium

May 13 through May 15, 2024, at the Desmond Crowne Plaza located in Albany, New York

The 33rd IEEE Microelectronics Design & Test Symposium (MDTS, formerly known as NATW) provides an annual world forum for academia and industry. University faculty, student researchers, and industry engineers discuss latest advances in microelectronics, share their visions in modern microelectronic technologies, and foster academy-industry collaboration. The three-day symposium features keynote, invited talks, a panel and tutorial on the themes of **chipselets** and **hardware security**. Chipselets break large chip designs into smaller, ideally reusable, integrated circuits, and the Universal Chipset Interconnect Express (UCIE) standard addresses the challenges of connecting chipselets in the package. Hardware security for chip designs covers a broad range of issues, from preventing reverse engineering to blocking takeovers and data theft or manipulation.

MDTS 2024 is sponsored by IEEE Schenectady Section and IEEE Region 1, and is supported by Advantest Corporation, AdamsIP, Cadence Design Systems, Green Mountain Semiconductor, IBM Corporation, and co-promotion with the SWTest Conference.

Monday, May 13	
11:00 am - 8:00 pm	Registration
12:00 pm - 1:00 pm	Lunch
1:00 pm – 5:40 pm	MDTS Sessions
1:00 pm – 1:10pm	Welcome Address: Kelly Ockunzzi General Chair
Invited Speaker	
1:10 pm – 1:15 pm	Speaker Introduction
1:15 pm – 2:15 pm	Speaker: Aydin Aysu
Title: Emerging Security Challenges at the Junction of AI and Hardware	
Tutorial 2:15 - 5:40 PM : Chipselets and Hardware Security	
2:15 pm – 2:20 pm	Tutorialist Introduction:
2:20 pm – 3:20 pm	Speaker: Martin Cochet
Title: Everything you always wanted to know about UCIE	
3:20 pm – 3:30 pm	Break
3:30 pm – 3:35 pm	Tutorialist Introduction:
3:35 pm – 4:35 pm	Speaker: Ramesh Karri
Title: Chipselets for Security and Security of Chipselets	
4:35 pm – 4:40 pm	Tutorialist Introduction:
4:40 pm – 5:25 pm	Speaker: Paul Reuter
Title: IEEE P3405 Introduction, status update (Chipselet interconnect test and repair)	
6:00 pm – 7:30 pm	Opening Reception Dinner Buffet 5 Fort Orange
7:30 pm – 9:00 pm	Panel: “Rise of the Chipselets” - Design, Test and Hardware Security
Panel Chair: Malinky Ghosh Panel Moderator: Eugene Atwood	
Panelists	
Ramesh Karri, Professor, Electrical and Computer Engineering, New York University	
Martin Cochet, Senior Research Scientist, IBM Research	
Nathaniel Cady, Associate Dean, University at Albany, The State University of New York	
Paul Reuter, Senior Software Engineer, Siemens Digital Industries Software	

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Tuesday, May 14	
7:00 am - 6:00 pm	Registration
7:00 am - 8:30 am	Breakfast
8:30 am – 6:00 pm	MDTS Sessions
Session 1	
8:00 am - 8:05 am	Welcome: Kelly Ockunzzi General Chair
8:05 am – 8:10 am	Program Introduction: Uma Srinivasan Program Chair
Invited Speaker	
8:10 am – 8:15 am	Invited Speaker Introduction:
8:15 am – 9:10 am	Invited Speaker: John Oakley Title: NIST-SRC Microelectronic and Advanced Packaging Roadmap
Student Paper Session 1 & 2	
Session Chair:	
9:10 am - 9:30 am	Paper 1.1: Title: Investigating Security on Networks on Chip with Ring Topology
9:30 am - 9:50 am	Paper 1.2: Title: Integrating ReRAM for Neuromorphic Computing: Real-time testing of packaged 64x64 1T1R crossbar arrays using a custom build microcontroller board
9:50 am - 10:10 am	Paper 1.3 Title: Design of an OTA circuit for low voltage applications
10:10 am – 10:20 am	Break
10:20 am - 10:40 am	Paper 2.1 Title: Harmonic Tag with Probe-Fed Patch Antennas
10:40 am – 11:00 am:	Paper 2.2 Title: Advancing Track Detection and Safety Using LabVIEW
11:00 am – 11:05 am	Invited Speaker Introduction
11:05 am – 12:00 pm	Invited Speaker: Selçuk Köse Title: Side-channel Leakage in Superconducting Electronics: Foe or Friend?
12:00 pm - 1:00 pm	Lunch
Invited Speaker	
1:00 pm – 1:05 pm:	Invited Speaker: Introduction
1:05 pm – 2:00 pm:	Invited Speaker: Gordon Harling Title: Platforms for creating and integrating chiplets
Paper Session 3	
Session Chair:	
2:00 pm – 2:20 pm:	Paper 3.1 Title: Within-Chip Bridged-Pattern Short Detection Using Spatially Distributed Kerf Test Structures in 7nm FinFET Technology
2:20 pm - 2:40 pm	Paper 3.2: Title: On the Design of a 20 Channel Pin Parametric Measurement System for Post-Fabrication Testing
2:40 pm – 2:45 pm:	Invited Speaker: Introduction
2:45 pm – 3:40 pm:	Invited Speaker: Gordon Harling

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Title: Platforms for creating and integrating chiplets
Tour
3:40 pm – 5:40 pm: Albany Nanotech Tour
6:30 pm – 8:30 pm: Dinner and Recognition Event: Best Student Paper Award
8:30 pm - 10:00 pm Networking

Wednesday, May 15
7:00 am – 11:00 am Registration
7:00 am – 8:00 am Breakfast
8:00 am – 12:00 pm MDTS Sessions
8:00 am - 8:05 am Welcome: Kelly Ockunzzi General Chair
Invited Speaker
8:05 am – 8:10 am: Invited Speaker: Introduction
8:10 am – 9:05 am: Invited Speaker: Dean Sullivan
Title: “To break it, or fix it, that is the question”
Paper Session 4
Session Chair:
9:05 am – 9:25 am: Paper 4.1
Title: Machine Learning Infused Software Testing for Mobile Device Development
9:25 am – 9:45 am Paper 4.2
Title: Co-design of a Novel Highly Parallel Multi-Thousand Multi-Chip Neural Network Accelerator in 28nm CMOS
9:45 am – 10:05 am: Paper 4.3
Title: Gate Resistance Test Structures Bounded by Local Layout Density to Characterize Metal Gate Height Variation in 7nm FinFET Technology
10:05 am - 10:15 am Break
Paper Session 5
Session Chair:
10:15 am – 10:35 am Paper 5.1
Title: Imaging Resistant Mask Programmable Read Only Memory (ROM)
10:35 am – 10:55 am Paper 5.2
Title: High-Speed Receiver Transient Modeling with Generative Adversarial Networks
Invited Speaker
10:55 am – 11:00 am: Invited Speaker: Introduction
11:00 am – 11:50 am: Invited Speaker: Xiaolin Xu
Title: On the Dark Side of FPGA as A Cloud-Hardware Accelerator
11:50 am – 12:00 pm Closing Remarks, Andrew Laidler Vice General Chair
12:00 pm – 1:00 pm Lunch

Please complete our survey online:

[Microelectronic Design and Test Symposium 2024 Survey](#)

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