2024 IEEE Microelectronics Design and Test Symposium

May 13 through May 15, 2024, at the Desmond Crowne Plaza located in Albany, New York

The 33rd IEEE Microelectronics Design & Test Symposium (MDTS, formerly known as NATW) provides an annual world forum for academia and industry. University faculty, student researchers, and industry engineers discuss latest advances in microelectronics, share their visions in modern microelectronic technologies, and foster academy-industry collaboration. The three-day symposium features keynote, invited talks, a panel and tutorial on the themes of **chiplets** and **hardware security**. Chiplets break large chip designs into smaller, ideally reusable, integrated circuits, and the Universal Chiplet Interconnect Express (UCIe) standard addresses the challenges of connecting chiplets in the package. Hardware security for chip designs covers a broad range of issues, from preventing reverse engineering to blocking takeovers and data theft or manipulation.

MDTS 2024 is sponsored by IEEE Schenectady Section and IEEE Region 1, and is supported by Advantest Corporation, AdamsIP, Cadence Design Systems, Green Mountain Semiconductor, IBM Corporation, and co-promotion with the SWTest Conference.

Monday, May 13
11:00 am - 8:00 pm Registration (Fort Orange)
12:00 pm - 1:00 pm Lunch (Koi Pond)
1:00 pm – 5:40 pm MDTS Sessions (Shaker Room)
1:00 pm – 1:10pm **Welcome Address: Kelly Ockunzzi General Chair**
Invited Speaker
1:10 pm – 1:15 pm Speaker Introduction: Krishna Chakravardula, Cadence
1:15 pm – 2:15 pm Speaker: Aydin Aysu **Title:** Emerging Security Challenges at the Junction of AI and Hardware
Tutorial 2:15 - 5:40 PM : Chiplets and Hardware Security
2:15 pm – 2:20 pm Tutorialist Introduction: Krishna Chakravardula, Cadence
2:20 pm – 3:20 pm Speaker: Martin Cochet **Title:** Everything you always wanted to know about UCIe
3:20 pm – 3:30 pm Break (Beverage Service 2 - 3:30pm, Shaker Room)
3:30 pm – 3:35 pm Tutorialist Introduction: Krishna Chakravardula, Cadence
3:35 pm – 4:35 pm Speaker: Ramesh Karri **Title:** High-Level Approaches to Hardware and Embedded Security
4:35 pm – 4:40 pm Tutorialist Introduction: Krishna Chakravardula, Cadence
4:40 pm – 5:25 pm Speaker: Paul Reuter **Title:** IEEE P3405 Introduction, status update (Chiplet interconnect test and repair)
6:00 pm – 7:30 pm Opening Reception Dinner Buffet (Koi Pond)
7:30 pm – 9:00 pm **Panel: "Rise of the Chiplets" - Design, Test and Hardware Security**
Panel Chair: Malinky Ghosh Panel Moderator: Eugene Atwood
Panelists
Ramesh Karri, Professor, Electrical and Computer Engineering, New York University
Martin Cochet, Senior Research Scientist, IBM Research
Nathaniel Cady, Associate Dean, University at Albany, The State University of New York
Paul Reuter, Senior Software Engineer, Siemens Digital Industries Software

Tuesday, May 14

7:00 am - 6:00 pm Registration (Fort Orange)
7:00 am - 8:30 am Breakfast (food service 7-8:30am, Shaker Room)
8:30 am – 6:40 pm MDTS Sessions (Shaker Room)
Session 1
8:30 am - 8:35 am Welcome: Kelly Ockunzzi General Chair
8:35 am – 8:45 am Program Introduction: Uma Srinivasan Program Chair
Invited Speaker
8:45 am – 8:50 am **Invited Speaker** Introduction: Tian Xia, University of Vermont
8:50 am – 9:50 am Invited Speaker: John Oakley **Title:** SRC's Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap: Driving a New Era of Innovation in Semiconductors and Digital Twins
Student Paper Session 1
Session Chair: Tian Xia, University of Vermont
9:50 am - 10:10 am Paper 1.1: **Title:** Integrating ReRAM for Neuromorphic Computing: Real-time testing of packaged 64x64 1T1R crossbar arrays using a custom build microcontroller board **Author:** Jeelka Natwarbhai Solanki (University at Albany)
10:10 am – 10:25 am Break (Beverage Service 10 - 11:30am, Shaker Room)
10:25 am - 10:45 am Paper 1.2 (Remote) **Title:** Design of an OTA circuit for low voltage applications **Author:** Prasanta K. Ghosh (Syracuse University), Pushkar Mishra (Syracuse University)
10:45 am – 11:05 am: Paper 1.3 **Title:** Harmonic Tag with Probe-Fed Patch Antennas **Author:** Swarup Chakraborty (University of Vermont)
Paper Session 2
Session Chair: Paul Reuter, Siemens
11:05 am – 11:25 am: Paper 2.1 **Title:** Within-Chip Bridged-Pattern Short Detection Using Spatially Distributed Kerf Test Structures in 7nm FinFET Technology **Author:** Cheng-Yi Lin (International Business Machines Corp.)
11:25 pm - 11:45 pm Paper 2.2: **Title:** On the Design of a 20 Channel Pin Parametric Measurement System for Post-Fabrication Testing **Author:** Xiaozhe Fan (GlobalFoundries)
12:00 pm - 1:00 pm Lunch (Koi Pond)
1:00 pm – 1:05 pm **Invited Speaker** Introduction: Paul Reuter, Siemens
1:05 pm – 2:05 pm Invited Speaker: Gordon Harling **Title:** Platforms for Creating and Integrating Chiplets
2:05 pm – 2:10 pm: **Invited Speaker**: Introduction: Paul Reuter, Siemens
2:10 pm – 3:10 pm: Invited Speaker: Selçuk Köse **Title:** Side-channel Leakage in Superconducting Electronics: Foe or Friend?
3:10 – 3:40 pm Break (Beverage Service 2 - 3:30pm, Shaker Room)
3:40pm – 5:40pm Albany Nanotech Tour
6:30 pm – 8:30 pm: Dinner and Recognition Event: Best Student Paper Award

Wednesday, May 15
7:00 am – 11:00 am Registration (Fort Orange)

7:00 am – 8:00 am Breakfast (food service 7-8:30am, Shaker Room)
8:00 am – 12:00 pm MDTS Sessions (Shaker Room)
8:00 am - 8:05 am Welcome: Kelly Ockunzzi General Chair
Invited Speaker
8:05 am – 8:10 am: Invited Speaker: Introduction: Eric Hunt-Schroeder
8:10 am – 9:05 am: Invited Speaker: Dean Sullivan **Title:** "To break it, or fix it, that is the question"
Paper Session 3
Session Chair: Eric Hunt-Schroeder
9:05 am – 9:25 am: Paper 3.1 **Title:** Machine Learning Infused Software Testing for Mobile Device Development **Author:** Sunder Chakravarty (Zebra Technologies Corporation)
9:25 am – 9:45 am Paper 3.2 **Title:** Co-design of a Novel Highly Parallel Multi-Thousand Multi-Chip Neural Network Accelerator in 28nm CMOS **Author:** Ewan McNeil (Green Mountain Semiconductor)
9:45 am – 10:05 am: Paper 3.3 **Title:** Gate Resistance Test Structures Bounded by Local Layout Density to Characterize Metal Gate Height Variation in 7nm FinFET Technology **Author:** Justin Zhu (International Business Machines)
10:05 am - 10:15 am Break (Beverage Service 10 - 11:30am, Shaker Room)
Paper Session 4
Session Chair: : Eric Hunt-Schroeder
10:15 am – 10:35 am Paper 4.1 **Title:** Imaging Resistant Mask Programmable Read Only Memory (ROM) **Author:** Eric Hunt-Schroeder (Marvell)
10:35 am – 10:55 am Paper 4.2 **Title:** High-Speed Receiver Transient Modeling with Generative Adversarial Networks **Author:** Priyank Kashyap (Hewlett-Packard Enterprise)
Invited Speaker
10:55 am – 11:00 am: Invited Speaker: Introduction: Eric Hunt-Schroeder
11:00 am – 11:50 am: Invited Speaker: Xiaolin Xu **Title:** On the Dark Side of FPGA as A Cloud-Hardware Accelerator
11:50 am – 12:00 pm **Closing Remarks, Andrew Laidler Vice General Chair**
12:00 pm – 1:00 pm Lunch (Koi Pond)

Please complete our survey online:

Microelectronic Design and Test Symposium 2024 Survey