MDTS

Keynote Speakers

IEEE

May 19

Day 1

10:45 AM - 11:35 AM

EUROPEAN PILOT LINE APECS - ADVANCED PACKAGING AND HETEROGENEOUS INTEGRATION FOR ELECTRONIC COMPONENTS AND SYSTEMS

Abstract: The pilot line for “Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems” (APECS) marks a major leap forward in strengthening Europe’s semiconductor manufacturing capabilities and chiplet innovation as part of the EU Chips Act. By providing large industry players, SMEs, and start-ups with facilitated access to cutting edge technology, the APECS pilot line will establish a strong foundation for resilient and robust European semiconductor supply chains. Within APECS, the institutes collaborating in the Research Fab Microelectronics Germany (FMD) will work closely with European partners, to make a significant contribution to the European Union´s goal of enhancing its global competitiveness in semiconductor technologies. APECS will drive innovation in energy efficient AI, manufacturing, mobility, information and communications, neuromorphic and quantum computing. It focuses on heterogeneous integration, in particular on emerging chiplet technologies.

Bio: Dr. Wenke Weinreich joined the Fraunhofer Center Nanoelectronic Technologies for PhD on new high-ks for DRAM in 2006. In 2011, she became a senior scientist at Fraunhofer IPMS in the division CNT and continued the development of new high-k materials as well as their integration in MIM capacitors for memories and passive devices. Since 2016 she has led the group Energy Devices dealing with CMOS integrated Si-capacitors, Li-Ion batteries as well as piezo-, pyro- and thermoelectric energy harvesting and sensor concepts. In 2019, she took charge of the business unit IOT Components & Systems within CNT combining activities like low power sensors, power management, nanopatterning and RF as well as AI processors. In 2020, she became the director of the division CNT which combines two business units and a 300 mm cleanroom infrastructure. Since 2021, she has also been deputy director of Fraunhofer IPMS, and in 2022, she started to lead the Center for Advanced CMOS and Heterointegration in Saxony.

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Keynote Speakers

IEEE

May 19

Day 1

1:55 PM – 2:45 PM

REPQC: REVERSE ENGINEERING AND BACKDOORING HARDWARE ACCELERATORS FOR POST-QUANTUM CRYPTOGRAPHY

Abstract: Significant research efforts have been dedicated to designing cryptographic algorithms that are quantum-resistant. The motivation is clear: robust quantum computers, once available, will render current cryptographic standards vulnerable. Thus, we need new Post-Quantum Cryptography (PQC) algorithms, and, due to the inherent complexity of such algorithms, there is also a demand to accelerate them in hardware. In this talk, we show that PQC hardware accelerators can be backdoored by two different adversaries located in the chip supply chain. We propose REPQC, a sophisticated reverse engineering algorithm that can be employed to confidently identify hashing operations (i.e., Keccak) within the PQC accelerator - the location of which serves as an anchor for finding secret information to be leaked. From there, adversaries can mount diverse attacks, including backdoors and hardware trojans.

Keywords: Hardware Security, Reverse Engineering, Hardware Trojan Horses

Bio: Dr. Samuel Pagliarini received his PhD from Telecom ParisTech, Paris, France, in 2013. He has held research positions with the University of Bristol, Bristol, UK, and Carnegie Mellon University, Pittsburgh, PA, USA. From 2019 to 2023, he led the Centre for Hardware Security at Tallinn University of Technology in Tallinn, Estonia. He is currently a professor at Carnegie Mellon University, Pittsburgh, PA, USA.

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Keynote Speakers

IEEE

May 20

Day 2

8:15 AM – 9:15 AM

TOWARD AGILE AND INTELLIGENT ANALOG/RF IC DESIGN AUTOMATION

Abstract: Analog/RF IC design has long been a heavily manual process, from circuit topology generation, to sizing, and to layout. In the entire design process, extensive circuit simulations will be performed to check if various design constraints/objectives can be met and optimized. However, this design process is very tedious and not scalable. In this talk, I will present our recent and ongoing efforts toward agile and intelligent analog/RF IC design automation, from topology generation to device sizing and layout, and from surrogate modeling to inverse design, leveraging the recent AI advancement and optimizations. Our overarching goal is to build an end-to-end analog/RF IC design and optimization flow, like that for digital IC from RTL to GDS.

Keywords: Electronic Design Automation, AI/ML, Analog and RF IC

Bio: David Pan is a professor and holder of Silicon Laboratories Endowed Chair at the Chandra Department of Electrical and Computer Engineering, The University of Texas at Austin. His research interests include design automation for digital/analog/mixed-signal/RF ICs and emerging technologies, synergistic AI/IC co-optimizations, design and technology/system co-optimizations, etc. He has published over 500 refereed journal/conference papers and 9 US patents. He has served in many journal editorial boards and conference committees, e.g., as DAC 2024 TPC Chair and ICCAD 2019 General Chair. He has received many awards, including SRC Technical Excellence Award, 21 Best Paper Awards from premier EDA/chips venues, DAC Top 10 Author Award in Fifth Decade, among others. He has graduated 53 PhD students and postdocs who are now holding key academic and industry positions. He is a Fellow of ACM, IEEE, and SPIE.

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Keynote Speakers

IEEE

May 20

Day 2

9:25 AM - 10:25 AM

OPPORTUNITIES AND CHALLENGES IN THE ERA OF CHIPLETS

Abstract: While chiplets give us many advantages such as Scalability, Flexibility, Improved yields, customization, re-usability of IP, it also faces challenges in the areas of design and integration complexity, latency in inter-chiplet communication, increased Power consumption, thermal challenges, and last but not least challenges associated with testing and validation. Furthermore standardization, what will be the real enabler of the open Chiplet economy, is still not mature. If our end goal is an open chiplet economy where all vendors small or big can sell their technology, we are far from it today. Chiplets today are being created by single vendors using their own proprietary interfaces. Currently, there is a lack of industry-wide standards for chiplet design and interconnects, leading to compatibility issues across different vendors. The Universal Chiplet Interconnect Express (UCIe) is a recent effort to address this but is still in its infancy.

Keywords: Heterogeneous Integration, Chiplet Ecosystem, Design and Integration Complexity, Testing and Validation of Chiplets, Flexible SoC Design

Bio: Dr. Moitreyee Mukherjee Roy has 25 years of successful strategic leadership within the IT industry. She has delivered in challenging leadership positions, led groups of highly skilled professionals to complete many successful projects across the globe; USA, Singapore, China, and India. Her experience ranges from Semiconductor R&D, Microprocessor design, research lab management, Product management, and IP strategy. She has started from ground zero and established new technical competencies in IBM and led them to own key global responsibilities both in production as well as R&D. Currently her focus is on Heterogenous Integration and Chiplets. Her key responsibilities are chiplet ecosystem build and business planning, Benchmarking, and IP strategy. She has contributed to technical committees of SPIE, ECS, and now IEEE. She currently chairs the IEEE Technical committee on Chiplets. She has a Ph.D in EE from NUS Singapore with 42 publications and 15 US patents.

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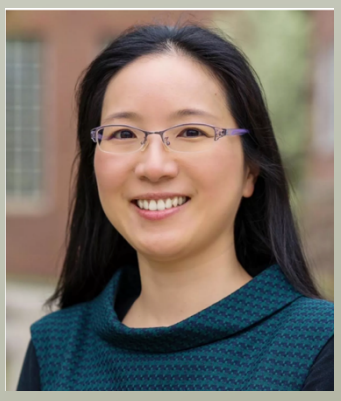
Keynote Speakers

IEEE

May 21

Day 3

8:00 AM - 8:50 AM



RESEARCH AND EDUCATION OPPORTUNITIES IN NSF SATC PROGRAMS

Abstract: While chiplets give us many advantages such as Scalability, Flexibility, Improved yields, customization, re-usability of IP, it also faces challenges in the areas of design and integration complexity, latency in inter-chiplet communication, increased Power consumption, thermal challenges, and last but not least challenges associated with testing and validation. Furthermore standardization, what will be the real enabler of the open Chiplet economy, is still not mature. If our end goal is an open chiplet economy where all vendors small or big can sell their technology, we are far from it today. Chiplets today are being created by single vendors using their own proprietary interfaces. Currently, there is a lack of industry-wide standards for chiplet design and interconnects, leading to compatibility issues across different vendors. The Universal Chiplet Interconnect Express (UCIe) is a recent effort to address this but is still in its infancy.

Bio: Dr. Qiaoyan Yu is a Program Director at the Division of Computer and Information Science & Engineering (CISE), Secure & Trustworthy Cyberspace (SaTC) Program. She is also a Professor of Electrical and Computer Engineering at the University of New Hampshire, where she directs the Reliable & Secure VLSI Systems Laboratory and the New Hampshire Cyber Security Enhanced Education Laboratory (NHCyberSEE Lab). Dr. Yu received her Ph.D. in Electrical and Computer Engineering from the University of Rochester (2011). Dr. Yu's research expertise includes hardware security with special emphases on approximate computing security, integrated circuit security, FPGA security, embedded system security, Internet-of-Things (IoT) security, and Networks-on-Chip architecture for fault tolerance and error management.

Dr. Yu received the NSF CAREER Award and the Air Force Research Lab Faculty Fellowship in 2017. Her work was also supported by Semiconductor Research Corporation (SRC) and UNH NSF Nanomanufacturing Center. She received the Best Poster Award at GLSVLSI'24, ISVLSI'16, Best Paper Award Finalist in MWSCAS'15, Best Paper Award Finalist in NOCS'11. She received the Excellence in Teaching Award at UNH in 2015. She has served on the technical program committees of HOST, Asian HOST, DAC, ASP-DAC, GLSVLSI, ISVLSI, DFT, ISCAS, MWSCAS, and ICCD.